

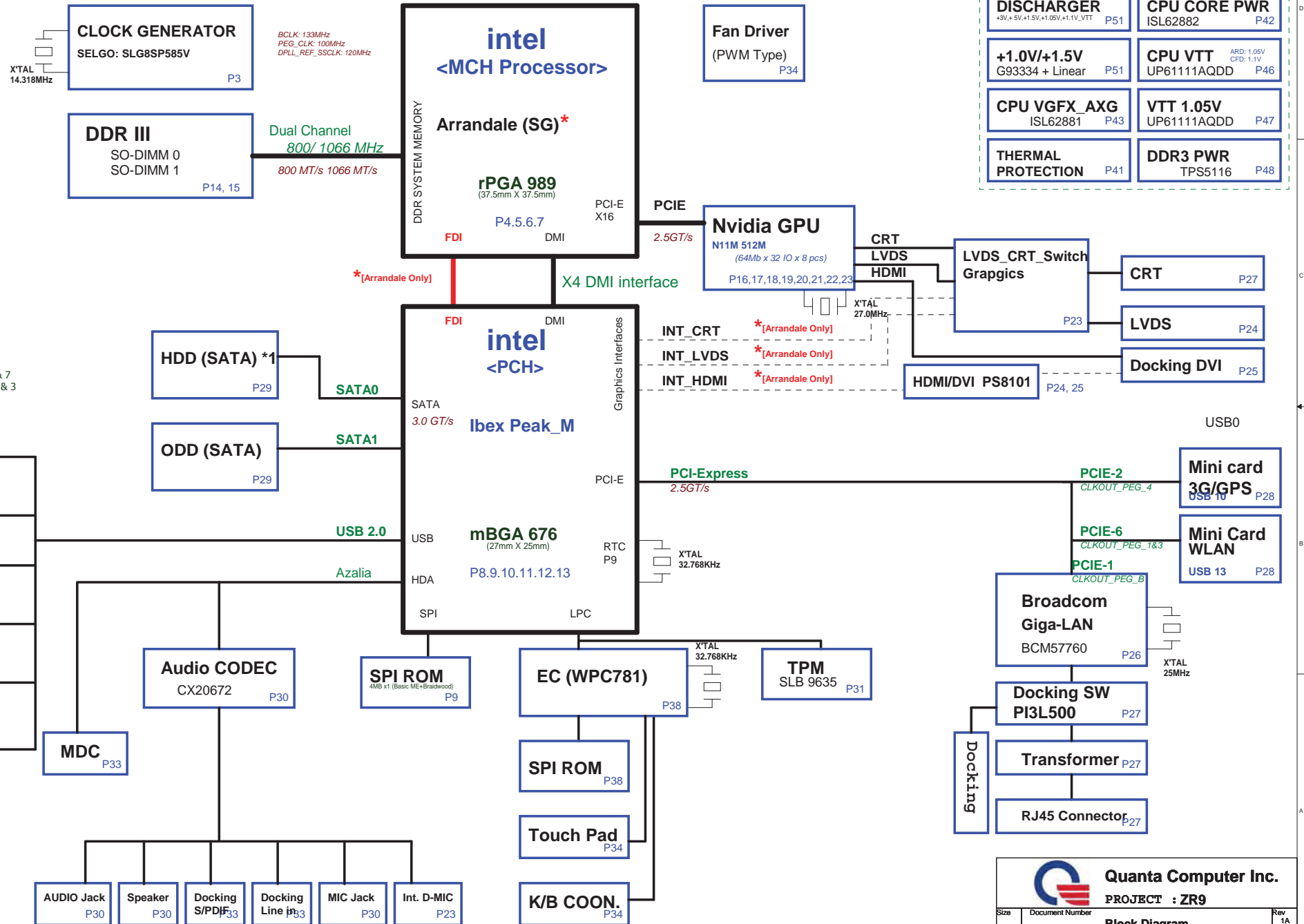
# ZR9 BLOCK DIAGRAM

SW@ --> iGPU & GPU Switch  
IV@ --> iGPU only  
EV@ --> GPU only  
SNP@ --> GPU N11P only  
SNM@ --> GPU N11M only  
CSP@ --> Operation P/N

Optional  
DOCKING

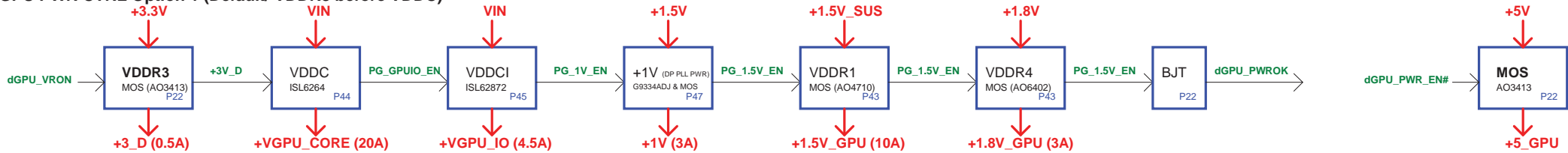
DVI  
VGA  
RJ45  
USB4  
AC JACK  
AUDIO/SPDIF  
MIC / LINE-IN

Note:  
HM55 does not support USB 6 & 7  
HM55 does not support SATA 2 & 3

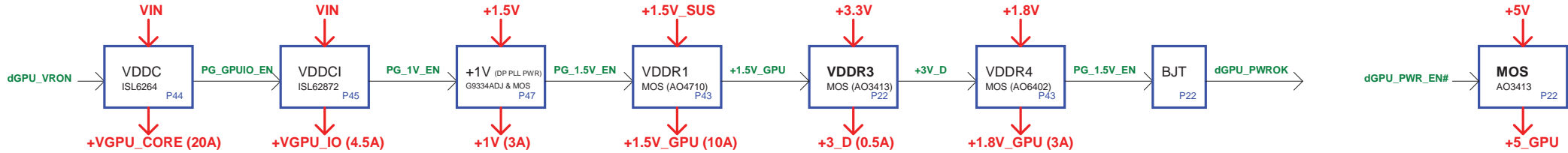




GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDR1)



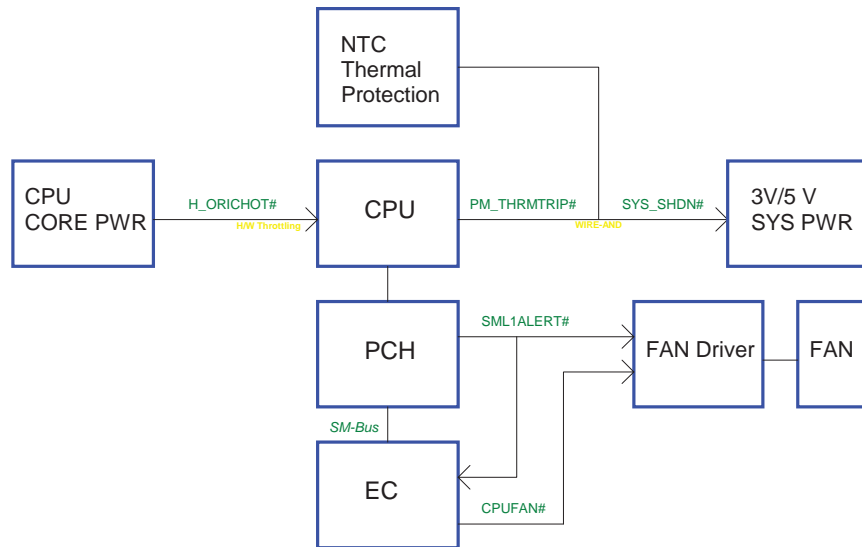
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



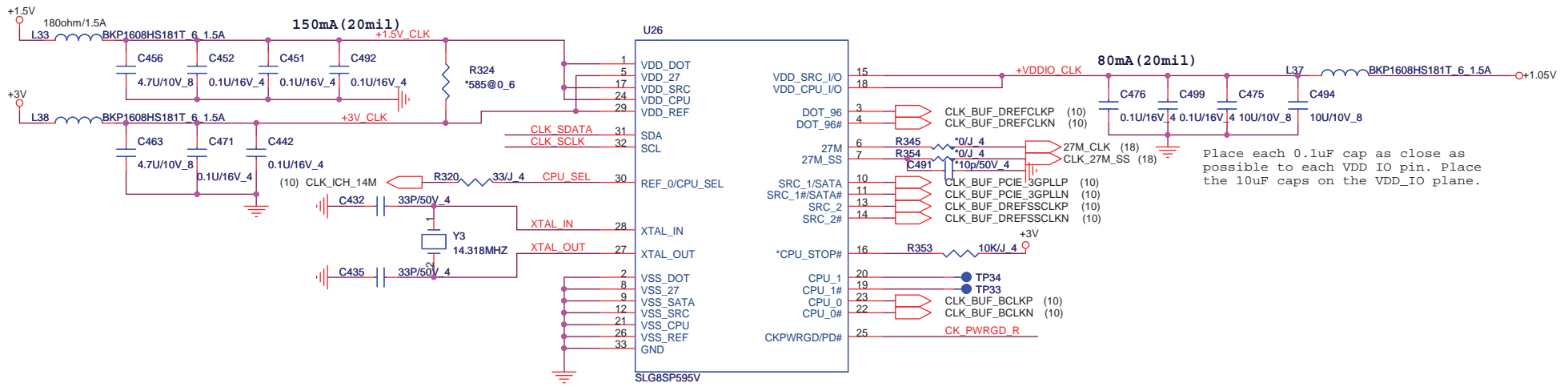
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

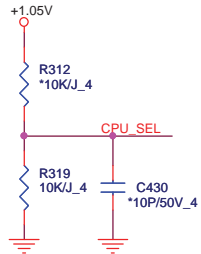
Thermal Follow Chart





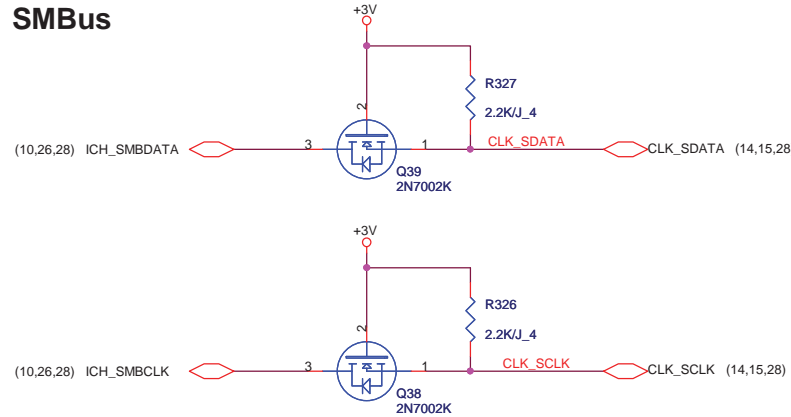


## CPU\_CLK select

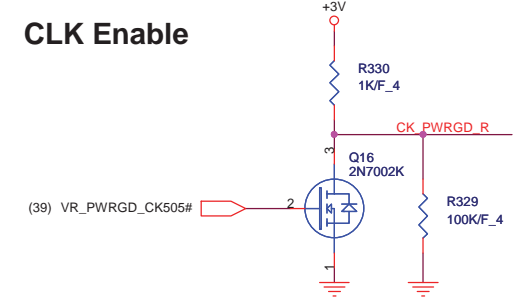


CPU_SEL	0	1
CPU0/1=133MHz (default)		CPU0/1=100MHz

## SMBus



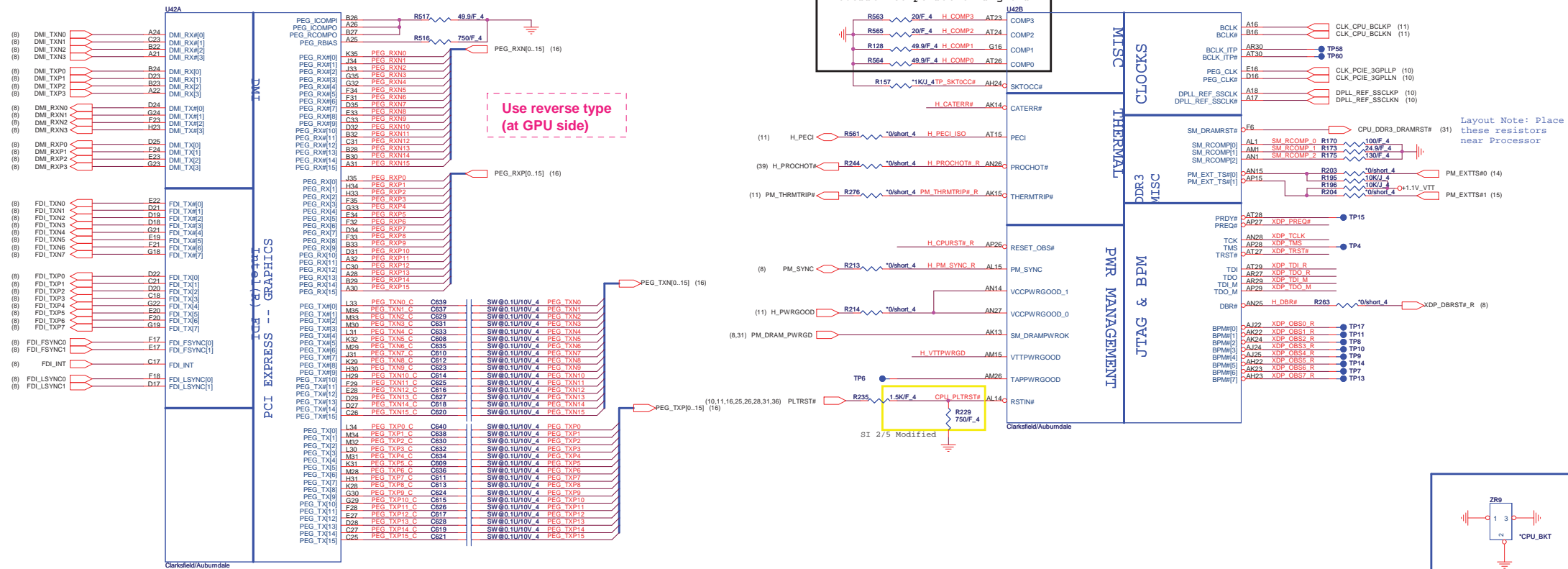
## CLK Enable



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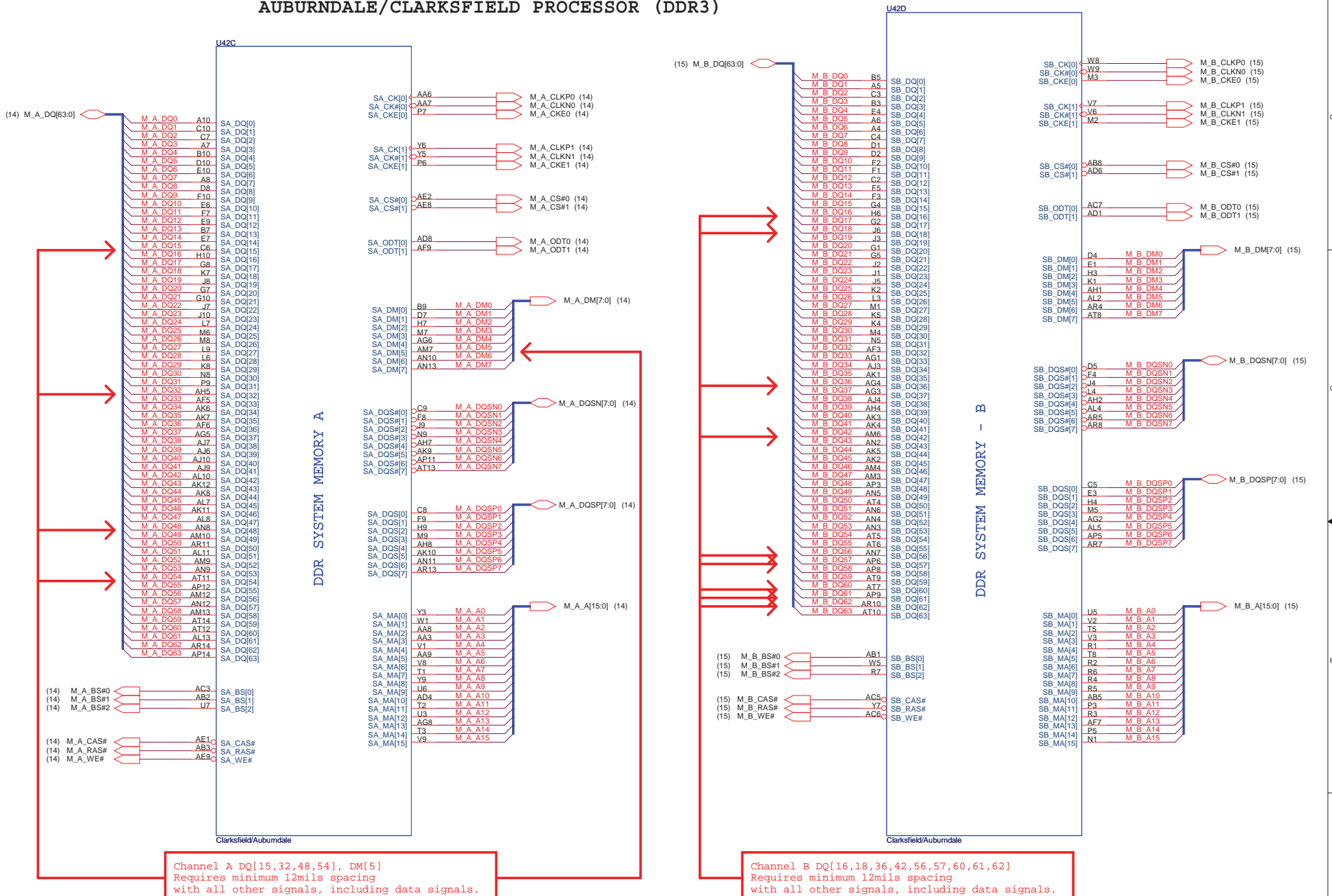
Size	Document Number	Rev
	<b>Clock Generator</b>	1A
Date:	Thursday, May 06, 2010	Sheet 3 of 47







# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



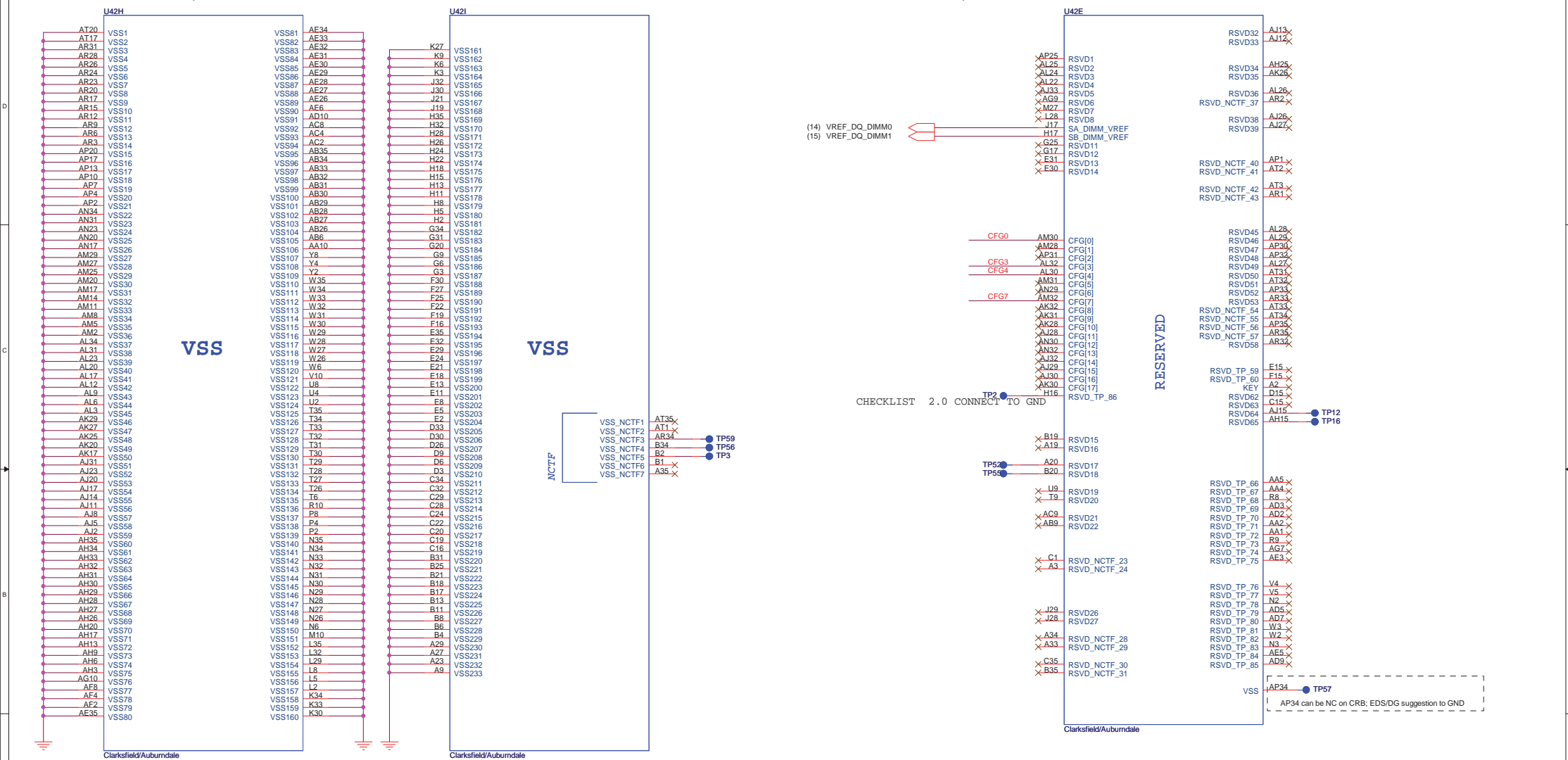






## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

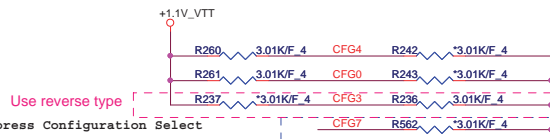
## AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



## Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[ 1:0 ] - PCI\_Epress Configuration Select  
\* 11= 1 x 16 PEG  
\* 10= 2 x 8 PEG



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. (ES1 only)

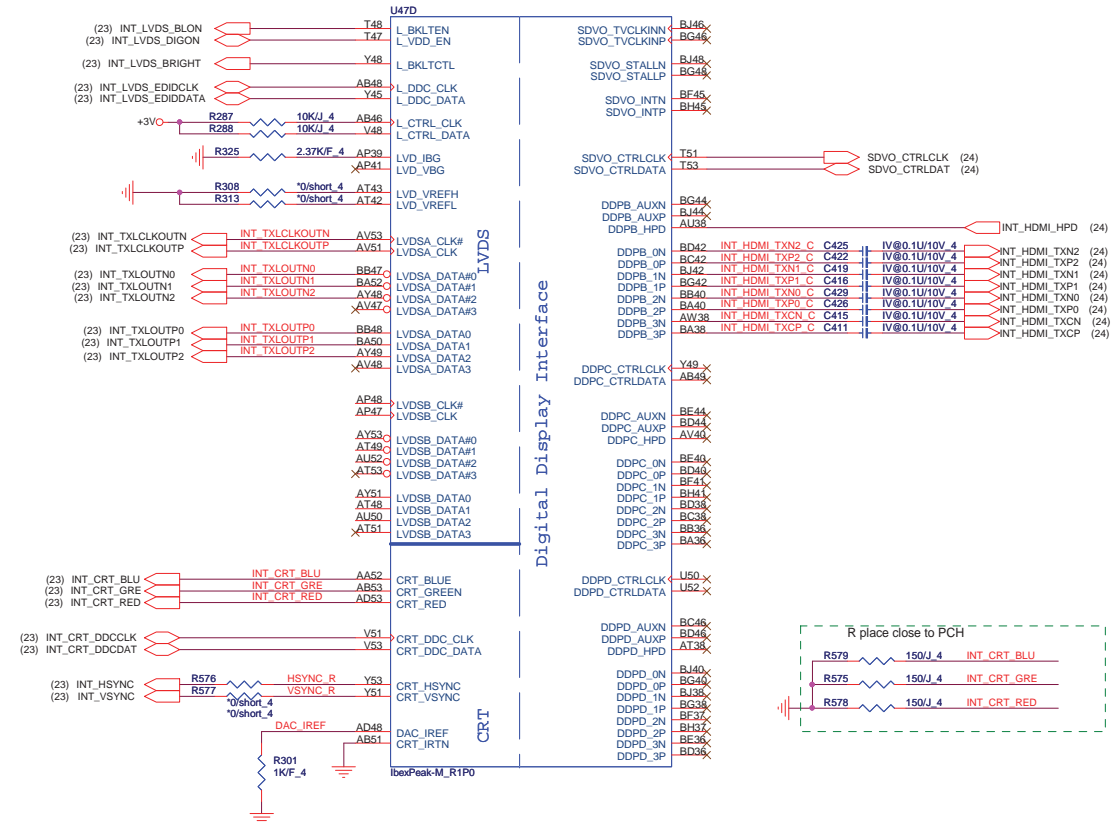


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PROJECT : ZR9

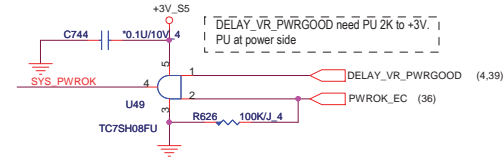
Size	Document Number	Rev
	AUBURND4 4/4	1A
Date:	Wednesday, May 05, 2010	Sheet 7 of 47



## IBEX PEAK-M (LVDS, DDI)



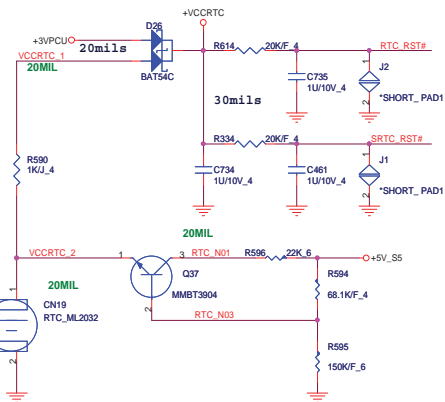
## System PWR\_OK



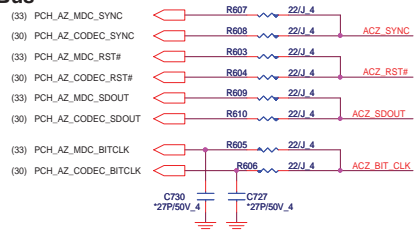
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## RTC Circuitry

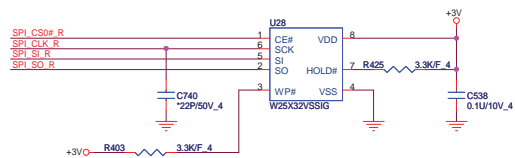


## HDA Bus

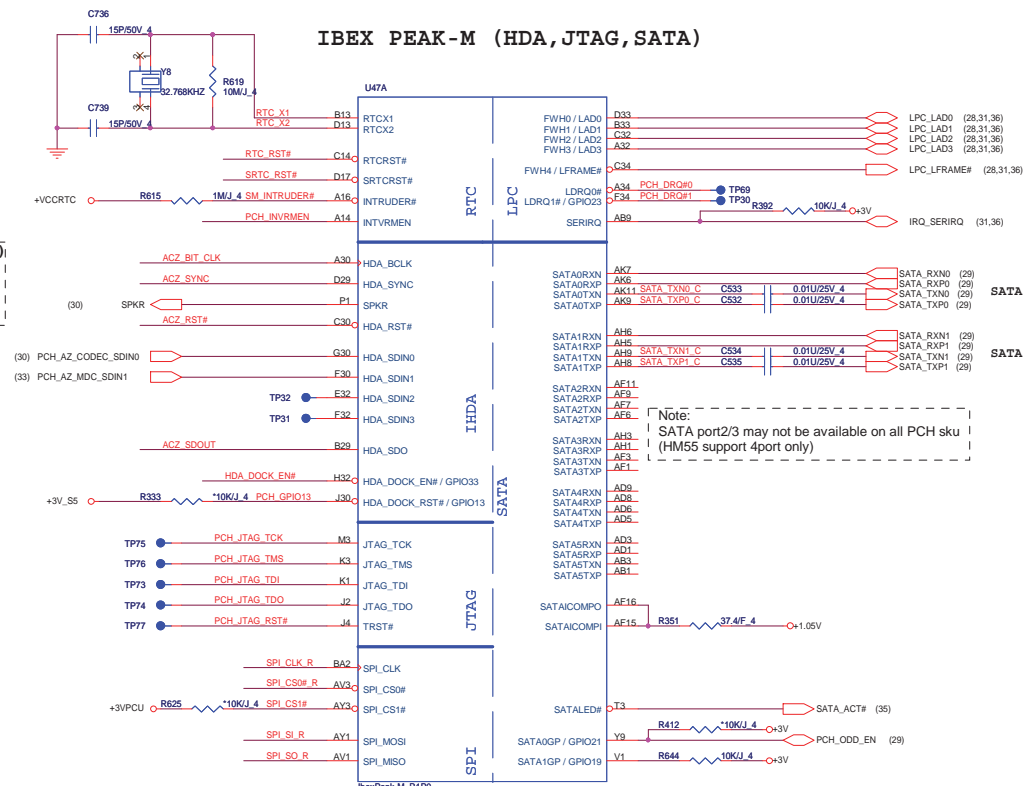


Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

## PCH SPI















## IBEX PEAK-M (HDA, JTAG, SATA)



### PCH Strap Table

BoxPeak-M\_R1P0

Pin Name	Strap description	Sampled	Configuration	ZY9B note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V  SPKR												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 R583 *4.7K 4 PCI_GNT3# (10)												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC  R616 330K/J 4 PCH_INVRMEN												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>1</td><td>0</td><td>PCI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	<b>Default weak pull-up on GNT0/1#</b> <b>[Need external pull-down for LPC BIOS]</b>  R286 *1K/J 4 R289 *1K/J 4 +3V R285 *1K/J 4 R300 *1K/J 4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESi strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	 R307 *4.7K 4 PWM_SELECT# (10,2)												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V  R623 *1K/J 4 NV_ALE (10)												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V  R622 *1K/J 4 NV_CLE (10)												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	 R310 *1K/J 4 +3V R309 *10K/J 4 HDA_DOCK_EN#												
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V  R624 *1K/J 4 SPI_SI R												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_SS  R383 *10K/J 4 RSV_GPIO8 (11)												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	 R384 *10K/J 4 RSV_GPIO27 (11)												
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_SS  R414 *1K/J 4 CR_WAKE# (11)												



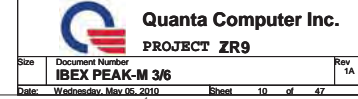
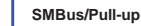
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**PROJECT : ZR9**

Size	Document Number	Rev
	<b>IBEX PEAK-M 2/6</b>	<b>1A</b>
Date:	Wednesday, May 05, 2010	Sheet 9 of 47



## IBEX PEAK-M (PCI-E, SMBUS, CLK)





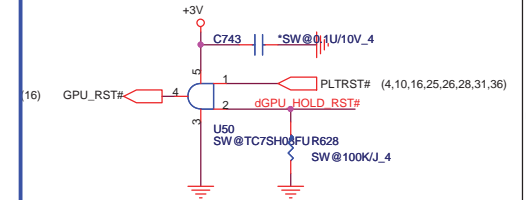
# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



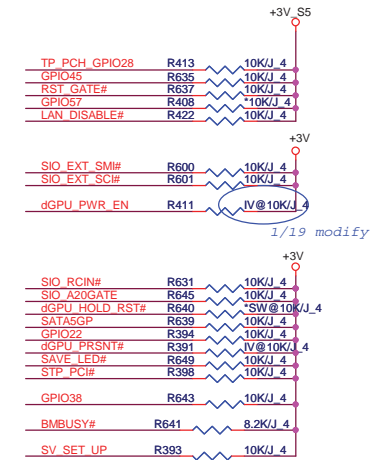
SATA5GP / GPIO49 / TEMP\_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

EC suggestion use GPIO49 for FAN control

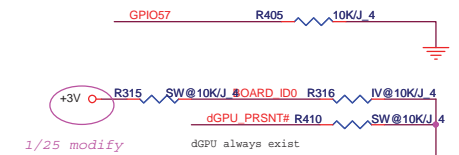
## GPU RST#



## GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------



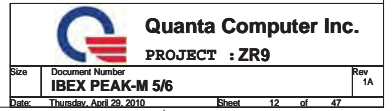
Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable



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**PROJECT : ZR9**

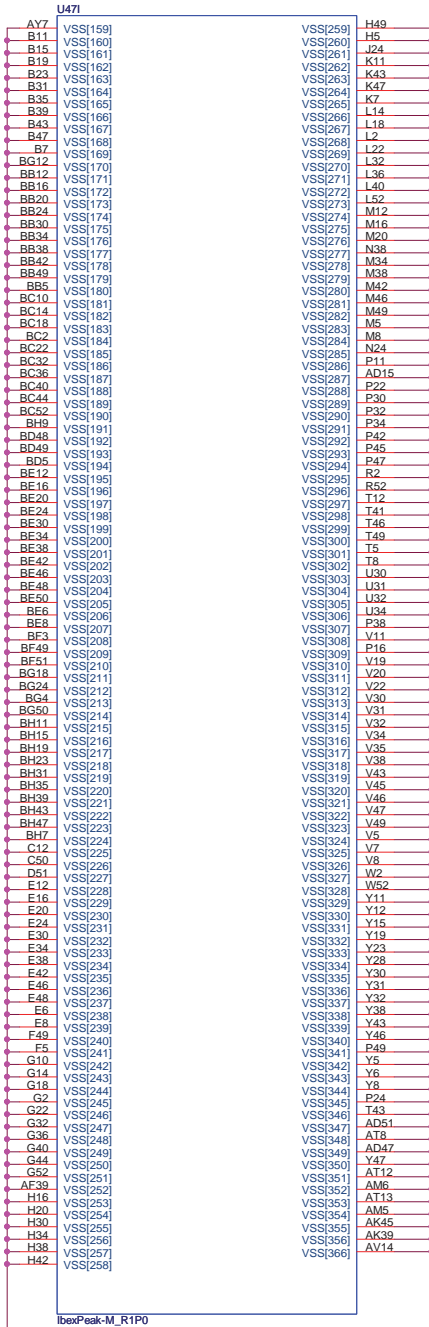
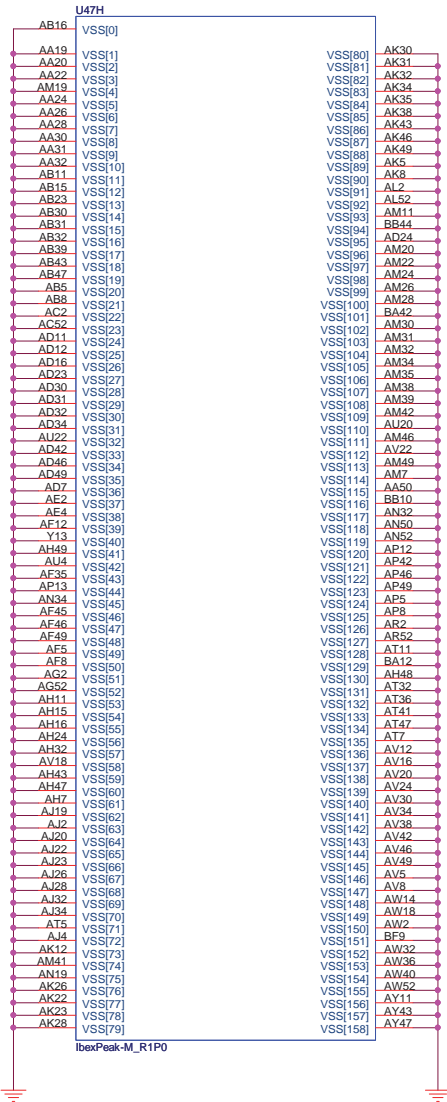


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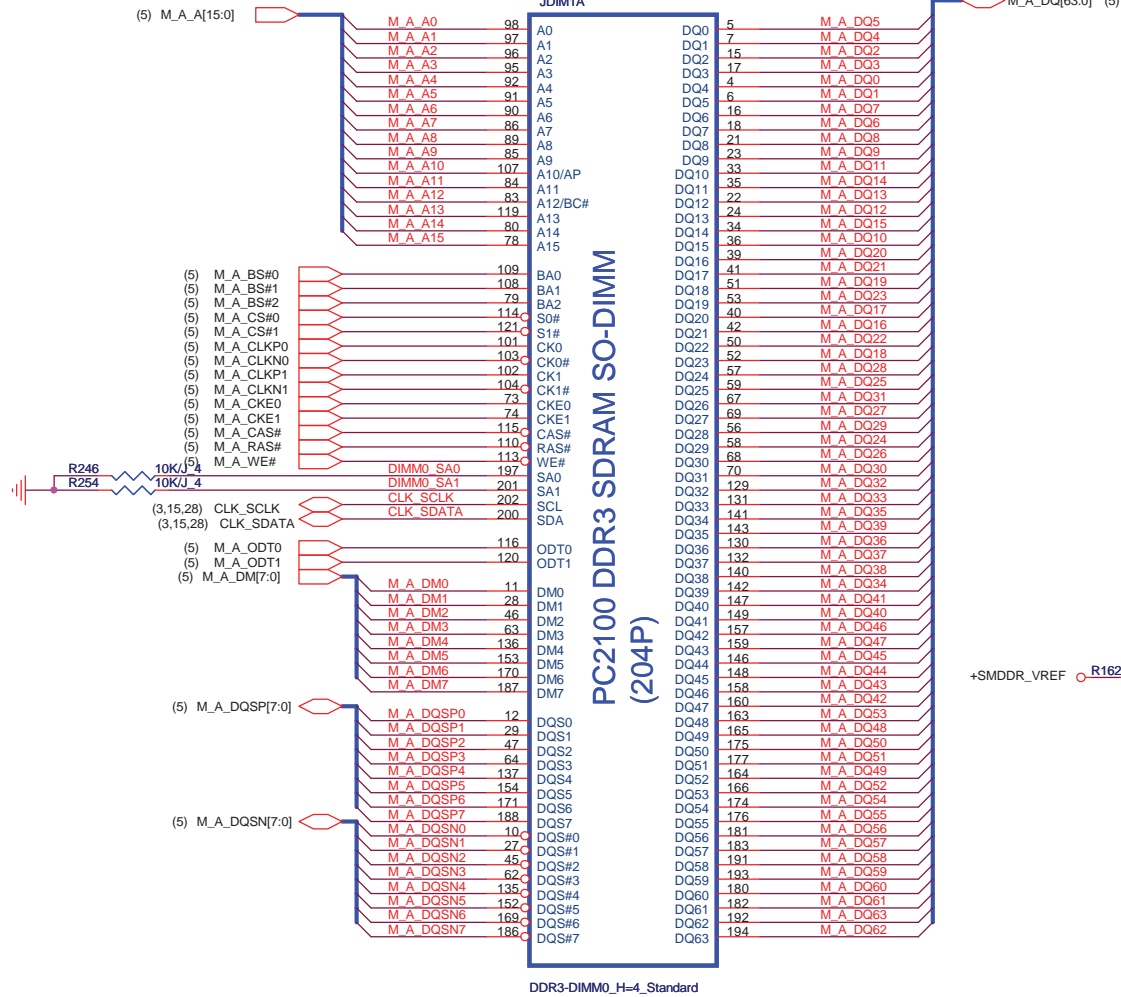




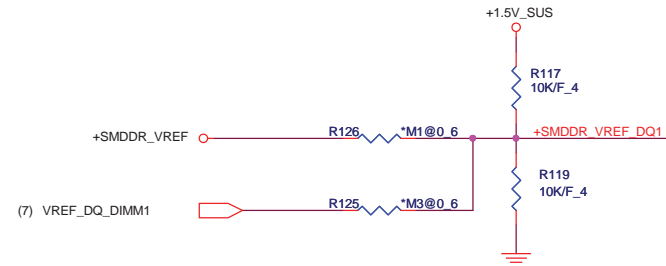
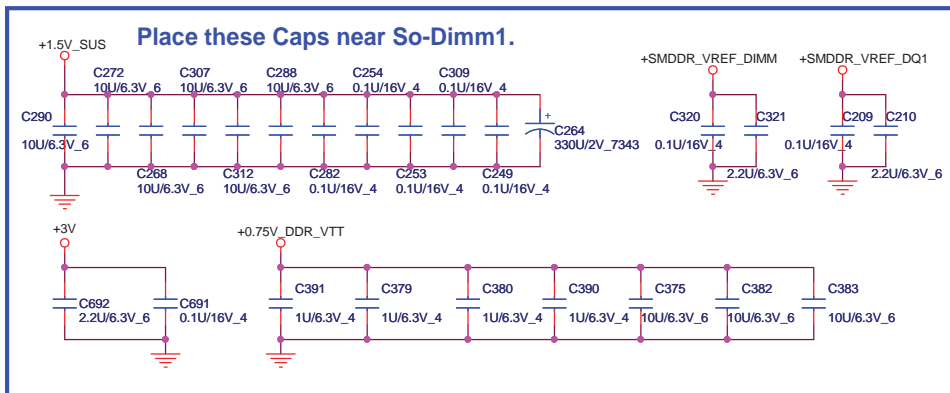
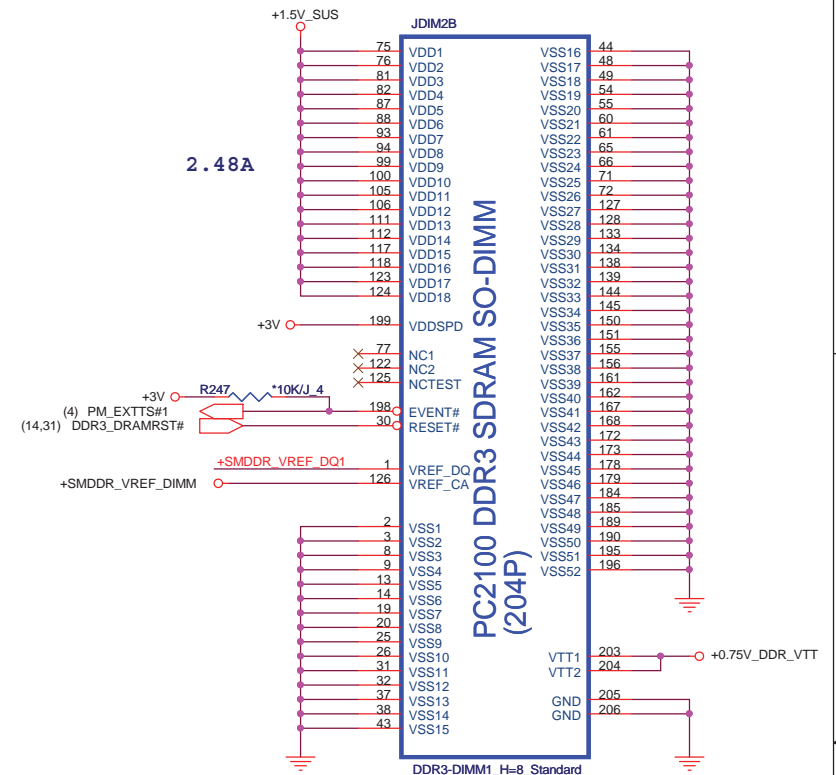
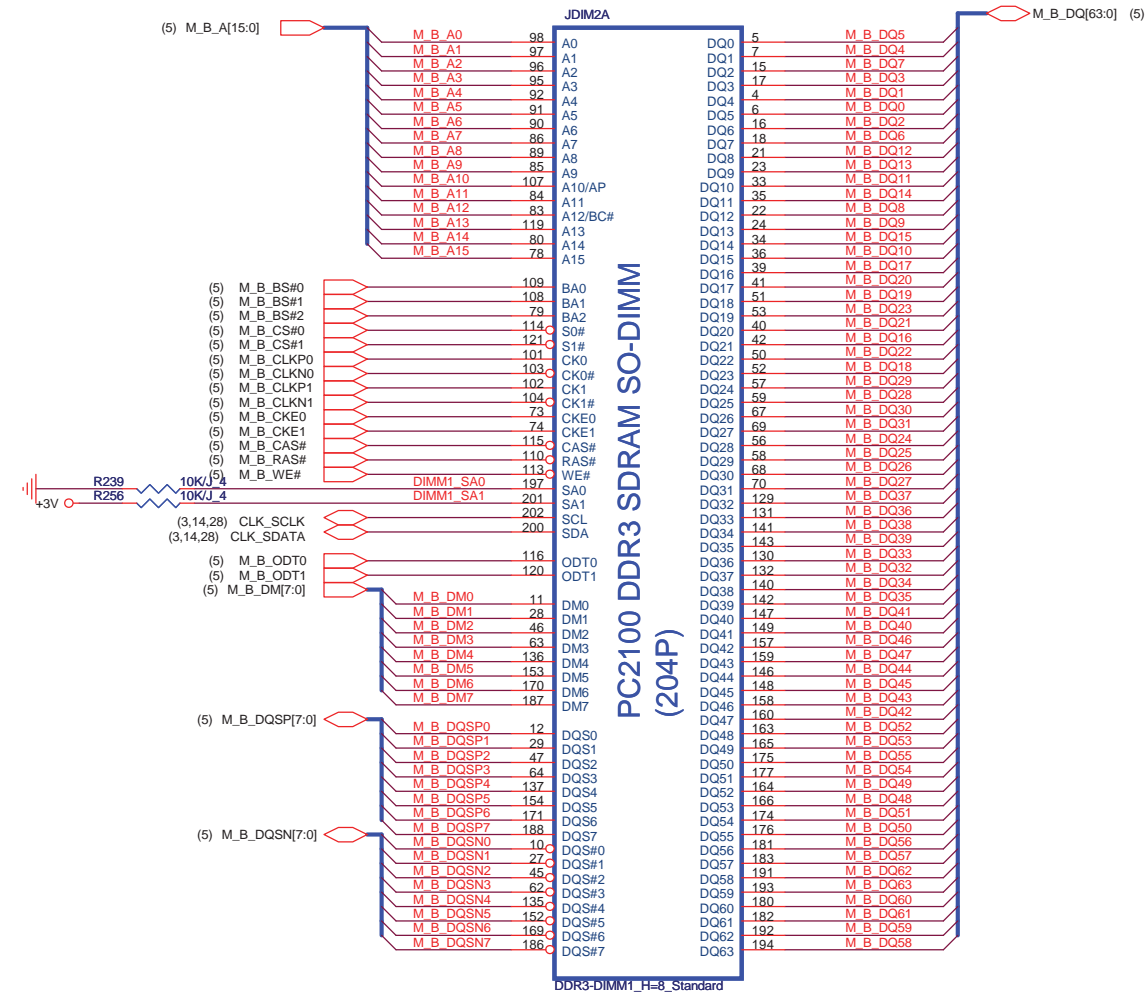
# IBEX PEAK-M (GND)







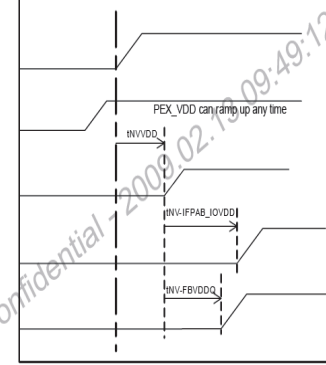
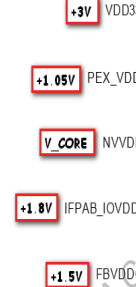






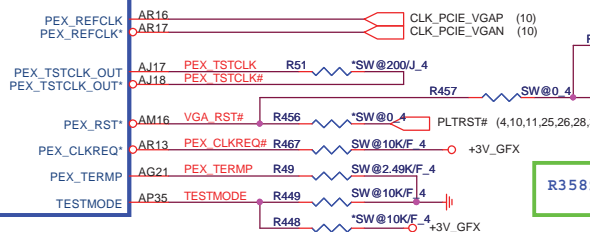
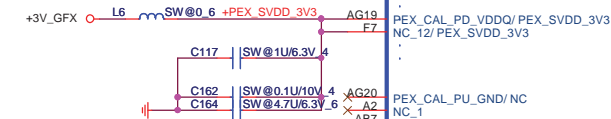
N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

## power up sequence



The diagram shows two signals: NVVDD and GPIO. The NVVDD signal starts at a low level, then ramps up to a higher level. The GPIO signal starts at a high level, then drops to a low level. A horizontal double-headed arrow labeled  $t_{sNVVDD} \leq 192\mu s$  indicates the time interval from the falling edge of the GPIO signal to the start of the NVVDD ramp.

Timing diagram for PEX\_RST deassertion. The diagram shows the I/O 3.3V signal (top) and the PEX\_RST signal (bottom). The PEX\_RST signal transitions from high to low, then back to high. The rising edge of PEX\_RST is marked with  $T_{rise} \geq 1\mu S$ . The falling edge of PEX\_RST is marked with  $T_{fail} \leq 500nS$ .

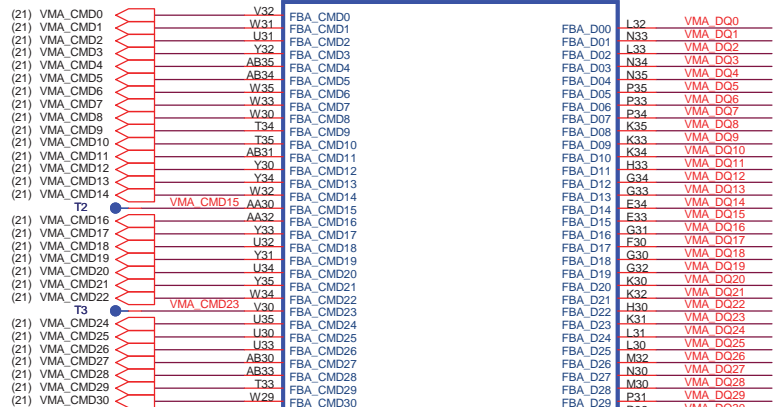


Only for Hybrid

Diagram illustrating a circuit configuration for a hybrid system, labeled "Only for Hybrid". The circuit includes a MOSFET (Q6, SW @ DTC144EUA) and a resistor (R80, SW @ 10K/F\_4) connected to a +3V\_GFX supply. The output of this stage is connected to another MOSFET (Q20, SW @ DTC144EUA) and a resistor (R489, SW @ 10K/F\_4), which is then connected to a +3V\_S5 supply. The output signal is labeled PEG\_CLKREQ# (10).



## U35B

fcbga073-nvidia-n11p-es-a1  
COMMON

VMA\_DM0 P32 FBA\_DM0  
VMA\_DM1 H34 FBA\_DM1  
VMA\_DM2 J30 FBA\_DM2  
VMA\_DM3 P30 FBA\_DM3  
VMA\_DM4 AF32 FBA\_DM4  
VMA\_DM5 AL32 FBA\_DM5  
VMA\_DM6 AL34 FBA\_DM6  
VMA\_DM7 AF35 FBA\_DM7

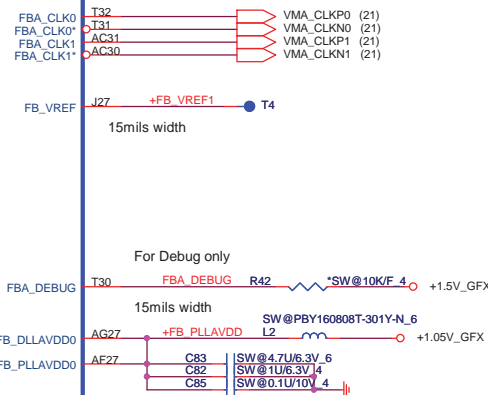
VMA\_WDQS0 L34 FBA\_DQS\_WP0  
VMA\_WDQS1 H35 FBA\_DQS\_WP1  
VMA\_WDQS2 J32 FBA\_DQS\_WP2  
VMA\_WDQS3 N31 FBA\_DQS\_WP3  
VMA\_WDQS4 AE31 FBA\_DQS\_WP4  
VMA\_WDQS5 AJ32 FBA\_DQS\_WP5  
VMA\_WDQS6 AJ34 FBA\_DQS\_WP6  
VMA\_WDQS7 AC33 FBA\_DQS\_WP7

VMA\_RDQS0 L35 FBA\_DQS\_RN0  
VMA\_RDQS1 G35 FBA\_DQS\_RN1  
VMA\_RDQS2 H31 FBA\_DQS\_RN2  
VMA\_RDQS3 N32 FBA\_DQS\_RN3  
VMA\_RDQS4 AD32 FBA\_DQS\_RN4  
VMA\_RDQS5 AJ31 FBA\_DQS\_RN5  
VMA\_RDQS6 AJ35 FBA\_DQS\_RN6  
VMA\_RDQS7 AC34 FBA\_DQS\_RN7

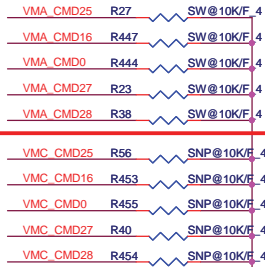
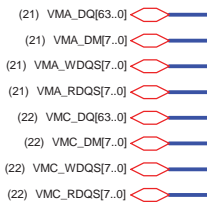
×P29 FBA\_WCK0  
×R29 FBA\_WCK0\_N  
×L29 FBA\_WCK1  
×M29 FBA\_WCK1\_N  
×G29 FBA\_WCK2  
×H29 FBA\_WCK2\_N  
×D29 FBA\_WCK3  
×E29 FBA\_WCK3\_N

AA27 FBVDDQ\_1  
AA29 FBVDDQ\_2  
AA31 FBVDDQ\_3  
AB27 FBVDDQ\_4  
AB29 FBVDDQ\_5  
AC27 FBVDDQ\_6  
AD27 FBVDDQ\_7  
AE27 FBVDDQ\_8  
AJ28 FBVDDQ\_9  
B18 FBVDDQ\_10  
E17 FBVDDQ\_11  
G17 FBVDDQ\_12  
G18 FBVDDQ\_13  
G22 FBVDDQ\_14  
G8 FBVDDQ\_15  
H29 FBVDDQ\_16  
J14 FBVDDQ\_17  
J15 FBVDDQ\_18  
J16 FBVDDQ\_19  
J17 FBVDDQ\_20  
J20 FBVDDQ\_21  
J21 FBVDDQ\_22  
J22 FBVDDQ\_23  
J23 FBVDDQ\_24  
J24 FBVDDQ\_25  
J29 FBVDDQ\_26  
J29 FBVDDQ\_27

## MEMORY I/F A

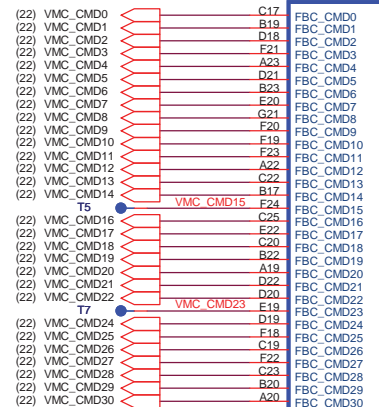


4/20 reserved for long run



Un-stuff for N11M  
Stuff for N11P, N11S

## U35C

fcbga073-nvidia-n11p-es-a1  
COMMON

VMC\_DM0 A16 FBC\_DM0  
VMC\_DM1 D10 FBC\_DM1  
VMC\_DM2 F11 FBC\_DM2  
VMC\_DM3 D15 FBC\_DM3  
VMC\_DM4 D27 FBC\_DM4  
VMC\_DM5 A34 FBC\_DM5  
VMC\_DM6 A34 FBC\_DM6  
VMC\_DM7 D28 FBC\_DM7

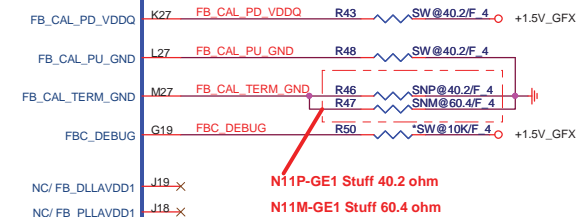
VMC\_WDQS0 G14 FBC\_DQS\_WP0  
VMC\_WDQS1 A10 FBC\_DQS\_WP1  
VMC\_WDQS2 E10 FBC\_DQS\_WP2  
VMC\_WDQS3 D14 FBC\_DQS\_WP3  
VMC\_WDQS4 E26 FBC\_DQS\_WP4  
VMC\_WDQS5 D32 FBC\_DQS\_WP5  
VMC\_WDQS6 A32 FBC\_DQS\_WP6  
VMC\_WDQS7 B26 FBC\_DQS\_WP7

VMC\_RDQS0 B14 FBC\_DQS\_RN0  
VMC\_RDQS1 B10 FBC\_DQS\_RN1  
VMC\_RDQS2 D9 FBC\_DQS\_RN2  
VMC\_RDQS3 E14 FBC\_DQS\_RN3  
VMC\_RDQS4 E26 FBC\_DQS\_RN4  
VMC\_RDQS5 D31 FBC\_DQS\_RN5  
VMC\_RDQS6 A31 FBC\_DQS\_RN6  
VMC\_RDQS7 A26 FBC\_DQS\_RN7

×G14 FBC\_WCK0  
×G15 FBC\_WCK0\_N  
×G11 FBC\_WCK1  
×G12 FBC\_WCK1\_N  
×G27 FBC\_WCK2  
×G28 FBC\_WCK2\_N  
×G24 FBC\_WCK3  
×G25 FBC\_WCK3\_N

N27 FBVDDQ\_28  
P27 FBVDDQ\_29  
R27 FBVDDQ\_30  
T27 FBVDDQ\_31  
U27 FBVDDQ\_32  
V27 FBVDDQ\_33  
V29 FBVDDQ\_34  
W27 FBVDDQ\_35  
W27 FBVDDQ\_36  
W27 FBVDDQ\_37  
Y27 FBVDDQ\_38

## MEMORY I/F C

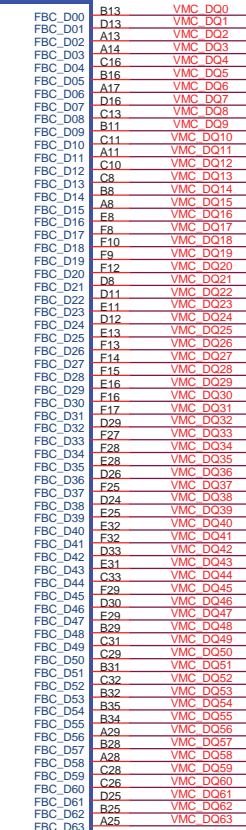


SW@ -&gt; IGPU &amp; GPU Switch

SNP@ -&gt; GPU N11P only

SNM@ -&gt; GPU N11M only

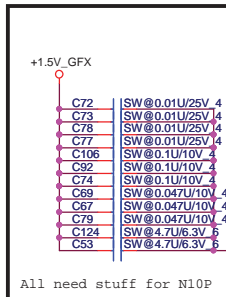
N11P	AJON11P0T19
N11M	AJON11M0T20



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PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (MEMORY I/F) 2/5	1A
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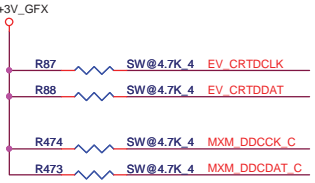
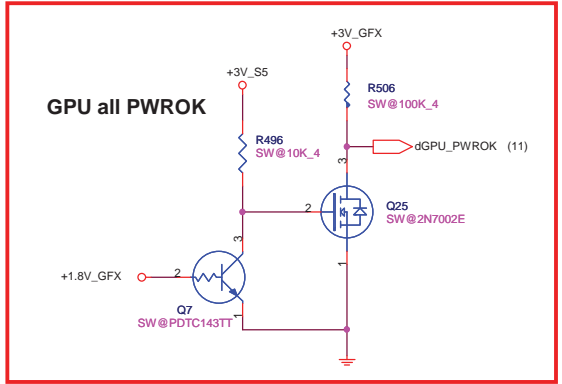
All need stuff for N10P




SW@ --> iGPU & GPU Switch  
SNP@ --> GPU N11P only  
SNM@ --> GPU N11M only

N11P	AJON11P0T19
N11M	AJON11M0T20

LVDS clk spread : Center  
+/-0.5% ( 30~33KHZ)



10 kΩ pull-down only if no spread chip used.



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	<b>N11P-GE (DISPLAY) 3/5</b>	1A
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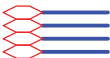






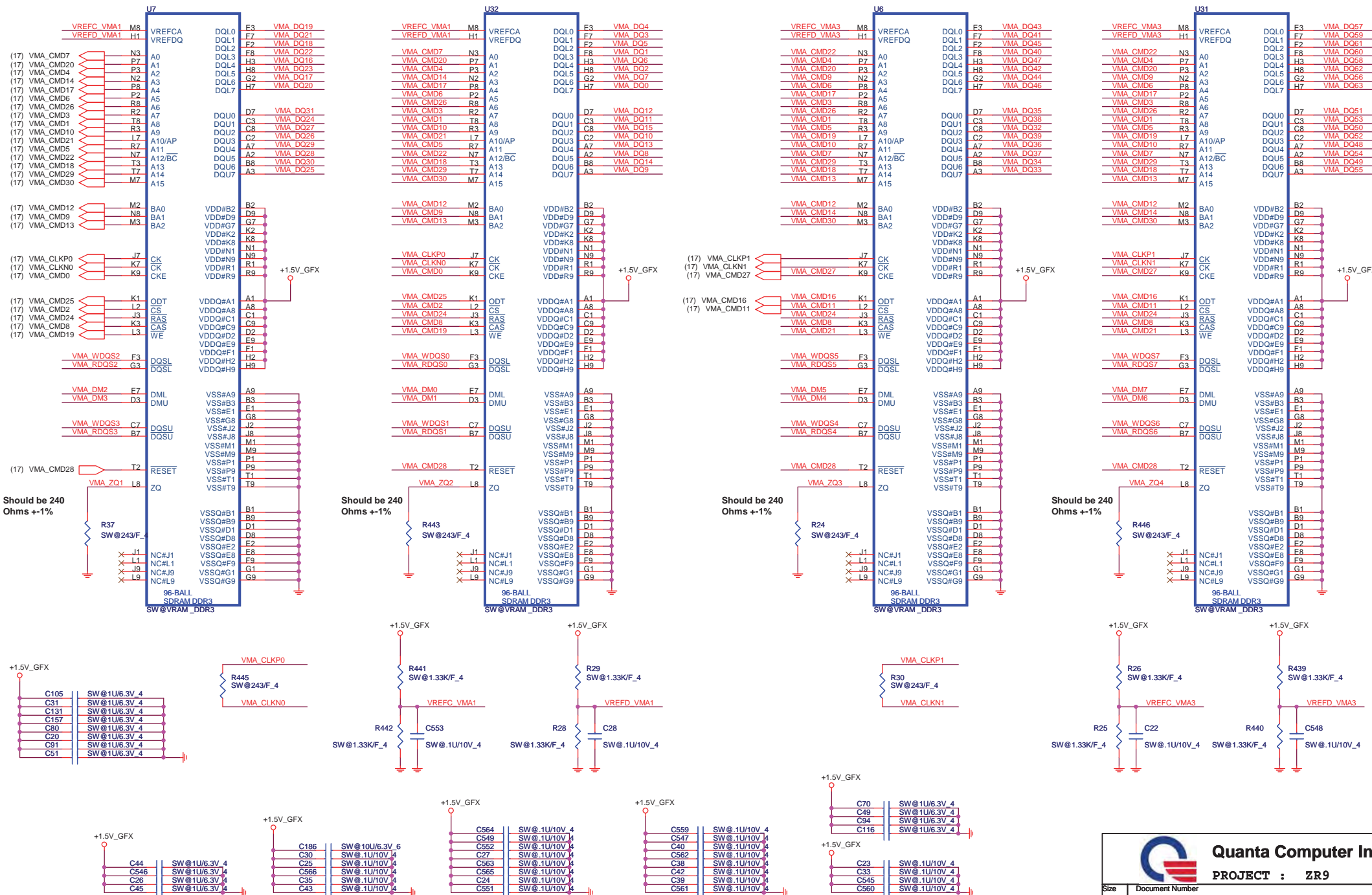
HYU	AKD5LZGTW04
SAM	AKD5LGGT506

```
(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]
```



**CHANNEL A: 256MB/512MB DDR3**

(17,22,45) +1.5V\_GFX

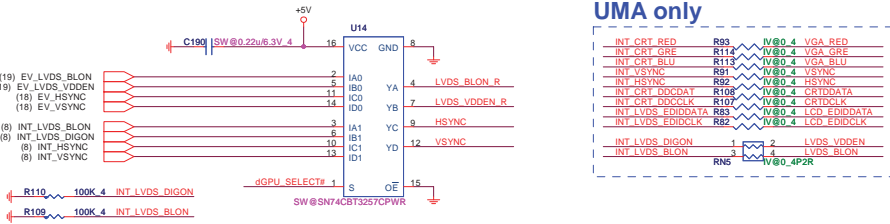




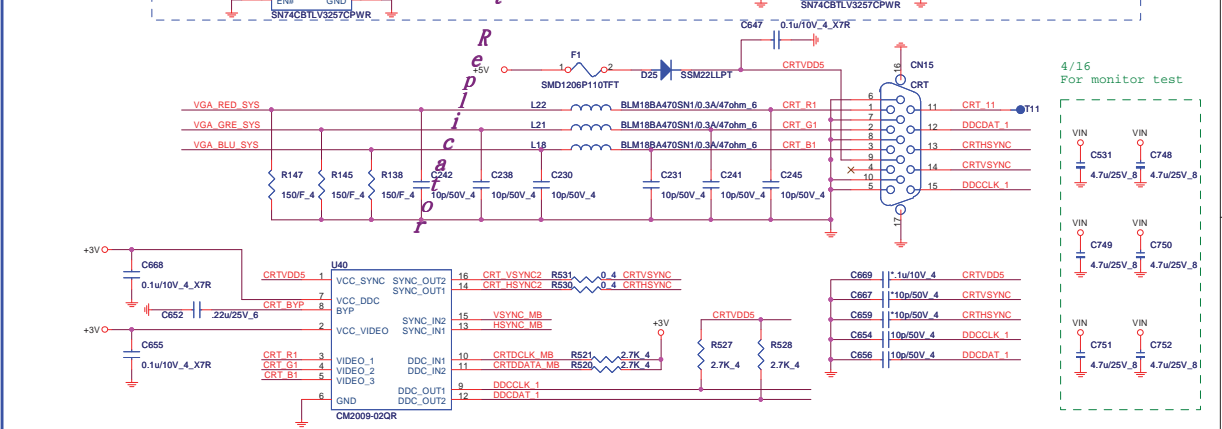
(17,21,45) +1.5V\_GFX 







(33) PR\_INSERT.



Signal	Pin	Function
(8) INT_TXLCLKOUTP	36	B2P
(8) INT_TXLCLKOUTN	34	B2N
(8) INT_TXLCLKOUTP2	33	B1P
(8) INT_TXLCLKOUTN2	32	B1N
(8) INT_TXLCLKOUTP1	30	B0P
(8) INT_TXLCLKOUTN1	29	B0N
(8) INT_TXLCLKOUTP0	28	B3P
(8) INT_TXLCLKOUTN0	27	B3N
	48	VDD
	36	VDD
	25	VDD
	21	VDD
	12	VDD
	4	VDD
	2	VDD
	13	dGPU_SELECT
	1	VSS
	3	VSS
	5	VSS
	7	VSS
	8	VSS
	11	VSS
	14	VSS
	17	VSS
	20	VSS
	22	VSS
	24	VSS
	26	VSS
	31	VSS
	37	VSS
	42	VSS
	47	VSS

SW @1000p/50V\_4

SW @1000p/50V\_4

C10 SW @2.2u/2.5V\_4

C11 SW @0.1u/10V\_4 X7R

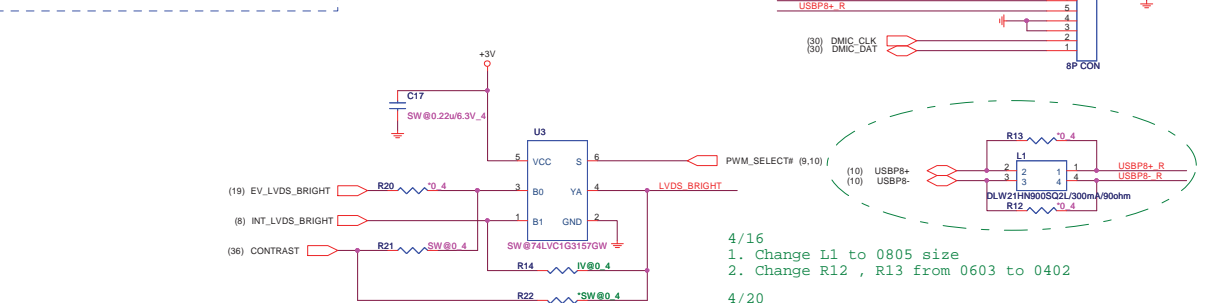
C12 SW @0.1u/10V\_4 X7R

C19 SW @2.2u/5.3V\_6

+1.8V

SW @TS30V42TD0VR

INT_TXLCLKOUTN	RN4	1	2	IV@0.4P2R	TXLCLKOUTN
INT_TXLCLKOUTP		3	4		TXLCLKOUTP
INT_TXLOUTN0	RN1	1	2	IV@0.4P2R	TXLOUTN0
INT_TXLOUTP0		3	4		TXLOUTP0
INT_TXLOUTN1	RN2	1	2	IV@0.4P2R	TXLOUTN1
INT_TXLOUTP1		3	4		TXLOUTP1
INT_TXLOUTN2	RN3	1	2	IV@0.4P2R	TXLOUTN2
INT_TXLOUTP2		3	4		TXLOUTP2



The diagram shows the electrical connection between an LCD module and the LVD-A305FVG+ driver. The LCD module is represented by a rectangular block with pins 1 through 30. The connections are as follows:

- Power and Ground:**
  - Pin 1 (3V) is connected to the LCDVCC supply.
  - Pin 2 (GND) is connected to the common ground.
  - Pin 3 (VIN) is connected to the system power supply.
  - Pin 4 (GND) is connected to the common ground.
  - Pin 5 (VIN) is connected to the system power supply.
  - Pin 6 (GND) is connected to the common ground.
  - Pin 7 (VIN) is connected to the system power supply.
  - Pin 8 (GND) is connected to the common ground.
  - Pin 9 (VIN) is connected to the system power supply.
  - Pin 10 (GND) is connected to the common ground.
  - Pin 11 (VIN) is connected to the system power supply.
  - Pin 12 (GND) is connected to the common ground.
  - Pin 13 (VIN) is connected to the system power supply.
  - Pin 14 (GND) is connected to the common ground.
  - Pin 15 (VIN) is connected to the system power supply.
  - Pin 16 (GND) is connected to the common ground.
  - Pin 17 (VIN) is connected to the system power supply.
  - Pin 18 (GND) is connected to the common ground.
  - Pin 19 (VIN) is connected to the system power supply.
  - Pin 20 (GND) is connected to the common ground.
  - Pin 21 (VIN) is connected to the system power supply.
  - Pin 22 (GND) is connected to the common ground.
  - Pin 23 (VIN) is connected to the system power supply.
  - Pin 24 (GND) is connected to the common ground.
  - Pin 25 (VIN) is connected to the system power supply.
  - Pin 26 (GND) is connected to the common ground.
  - Pin 27 (VIN) is connected to the system power supply.
  - Pin 28 (GND) is connected to the common ground.
  - Pin 29 (VIN) is connected to the system power supply.
  - Pin 30 (GND) is connected to the common ground.
- Signal Connections:**
  - Pin 3 (LCDVCC) is connected to the LCDVCC supply.
  - Pin 4 (GND) is connected to the common ground.
  - Pin 5 (LCD\_EIDCLK) is connected to the LCD\_EIDCLK signal.
  - Pin 6 (LCD\_EDD0DATA) is connected to the LCD\_EDD0DATA signal.
  - Pin 7 (TXL0OUTN) is connected to the TXL0OUTN signal.
  - Pin 8 (TXL0OUTP) is connected to the TXL0OUTP signal.
  - Pin 9 (TXL0OUTN1) is connected to the TXL0OUTN1 signal.
  - Pin 10 (TXL0OUTP1) is connected to the TXL0OUTP1 signal.
  - Pin 11 (TXL0OUTN2) is connected to the TXL0OUTN2 signal.
  - Pin 12 (TXL0OUTP2) is connected to the TXL0OUTP2 signal.
  - Pin 13 (TXLCLKOUTN) is connected to the TXLCLKOUTN signal.
  - Pin 14 (TXLCLKOUTP) is connected to the TXLCLKOUTP signal.
  - Pin 15 (PANEL\_COLOR\_CN) is connected to the PANEL\_COLOR\_CN signal.
  - Pin 16 (LVD5\_BRIGHT) is connected to the LVD5\_BRIGHT signal.
  - Pin 17 (BI\_ON) is connected to the BI\_ON signal.
  - Pin 18 (PANEL\_ENG\_CN) is connected to the PANEL\_ENG\_CN signal.
  - Pin 19 (INVCC0) is connected to the INVCC0 signal.
- Other Components:**
  - Resistor R10 (2.2K) is connected between pins 3 and 4.
  - Resistor R11 (2.2K) is connected between pins 4 and 5.
  - Resistor R9 (0.1ohm) is connected between pins 28 and 29.
  - Resistor R8 (0.1ohm) is connected between pins 29 and 30.
  - Capacitor C6 (0.1u/10V\_4\_X7R) is connected between pins 1 and 2.
  - Capacitor C5 (1000p/50V\_4) is connected between pins 3 and 4.
  - Capacitor C7 (4.7u/25V\_8) is connected between pins 5 and 6.
  - Capacitor C3 (1000p/50V\_4) is connected between pins 7 and 8.
  - TP41 and TP42 are test points located near the LCD module.

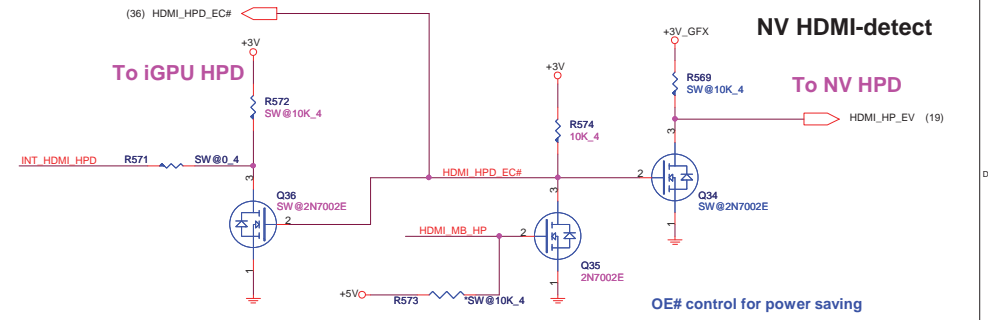
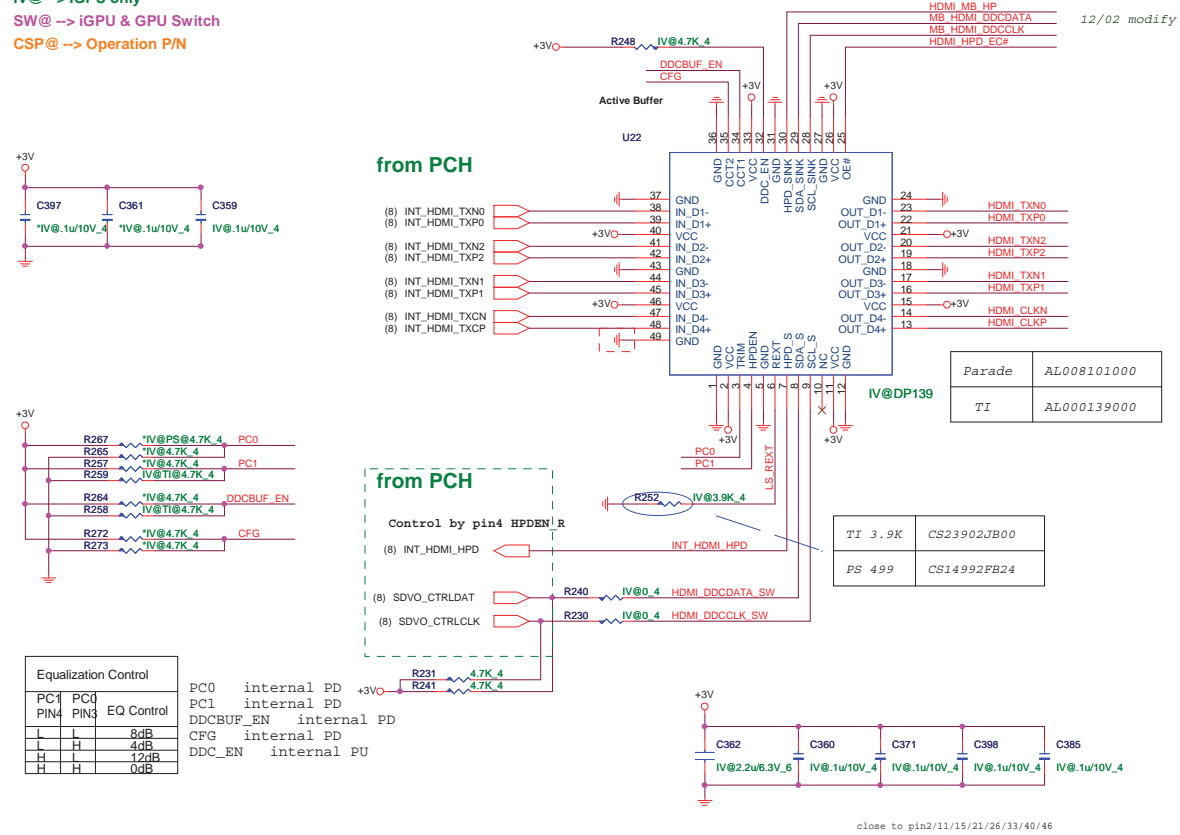
The LVD-A305FVG+ is shown as a multi-pin connector with pins 1 through 30. The connections are as follows:

- Pin 1 (GND) is connected to the common ground.
- Pin 2 (GND) is connected to the common ground.
- Pin 3 (GND) is connected to the common ground.
- Pin 4 (GND) is connected to the common ground.
- Pin 5 (GND) is connected to the common ground.
- Pin 6 (GND) is connected to the common ground.
- Pin 7 (GND) is connected to the common ground.
- Pin 8 (GND) is connected to the common ground.
- Pin 9 (GND) is connected to the common ground.
- Pin 10 (GND) is connected to the common ground.
- Pin 11 (GND) is connected to the common ground.
- Pin 12 (GND) is connected to the common ground.
- Pin 13 (GND) is connected to the common ground.
- Pin 14 (GND) is connected to the common ground.
- Pin 15 (GND) is connected to the common ground.
- Pin 16 (GND) is connected to the common ground.
- Pin 17 (GND) is connected to the common ground.
- Pin 18 (GND) is connected to the common ground.
- Pin 19 (GND) is connected to the common ground.
- Pin 20 (GND) is connected to the common ground.
- Pin 21 (GND) is connected to the common ground.
- Pin 22 (GND) is connected to the common ground.
- Pin 23 (GND) is connected to the common ground.
- Pin 24 (GND) is connected to the common ground.
- Pin 25 (GND) is connected to the common ground.
- Pin 26 (GND) is connected to the common ground.
- Pin 27 (GND) is connected to the common ground.
- Pin 28 (GND) is connected to the common ground.
- Pin 29 (GND) is connected to the common ground.
- Pin 30 (GND) is connected to the common ground.

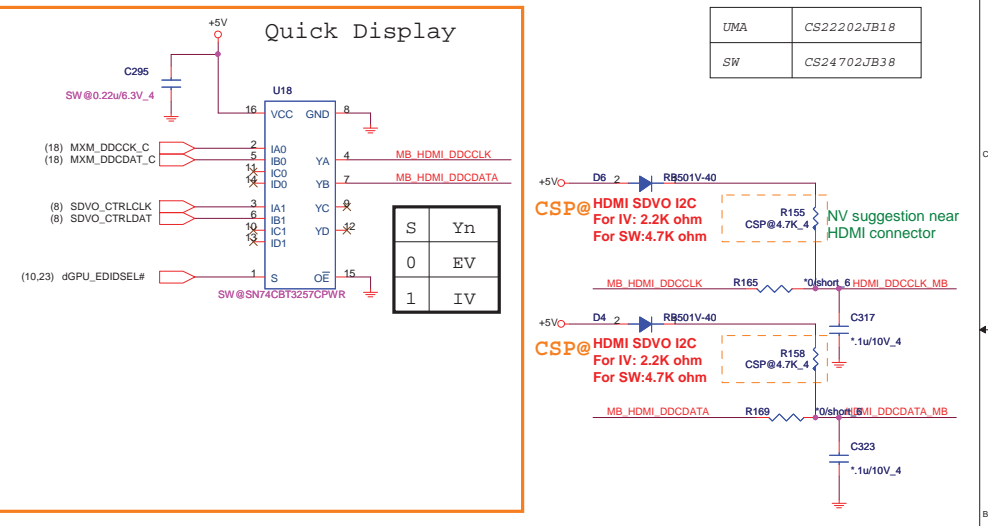


I@ HDMI LEVEL SHIFTER

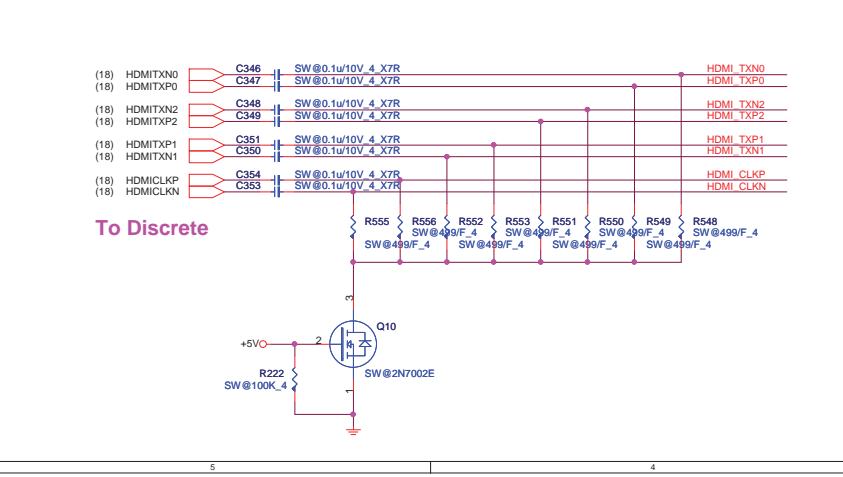
IV@ --> iGPU only  
SW@ --> iGPU & GPU Switch  
CSP@ --> Operation P/N



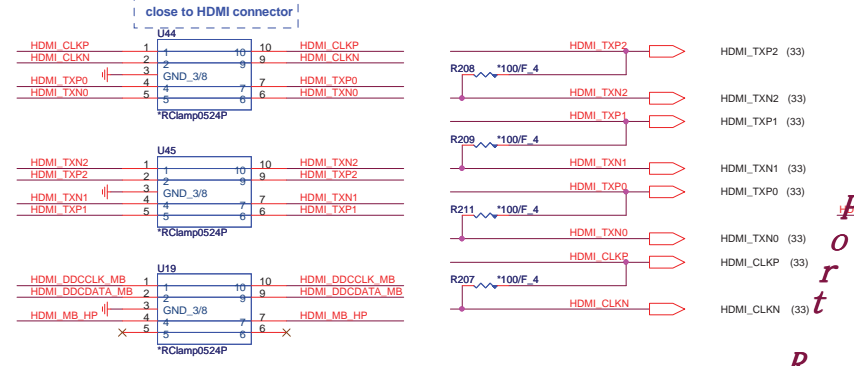
SDVO I2C Control



Switchable Graphic HDMI source



ESD Protect



Quanta Computer Inc.

PROJECT : ZR9

DVI (PS8101)

Size Document Number

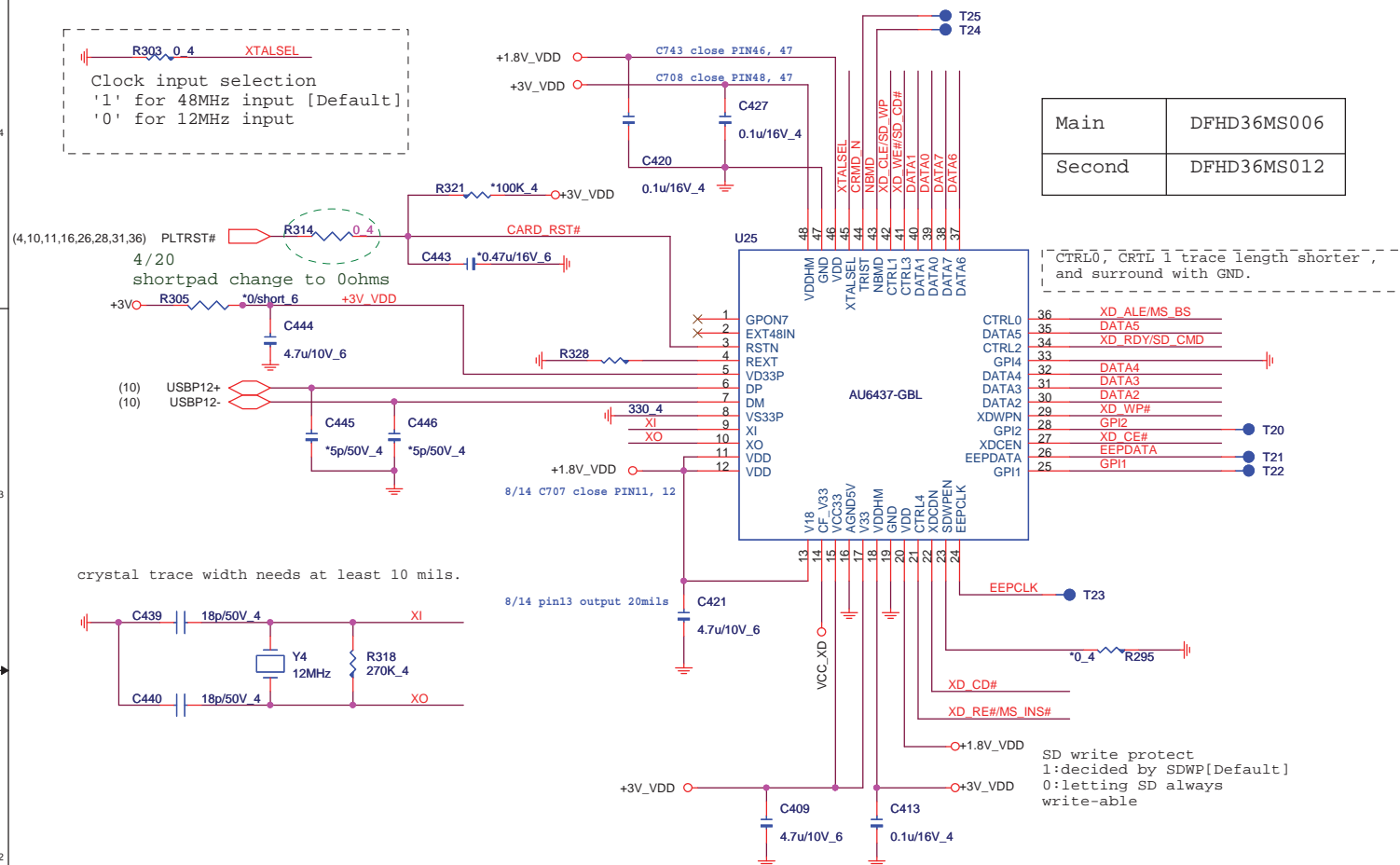
Date: Thursday, May 06, 2010

Rev 1A

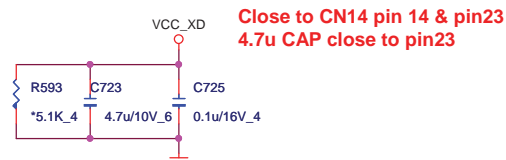
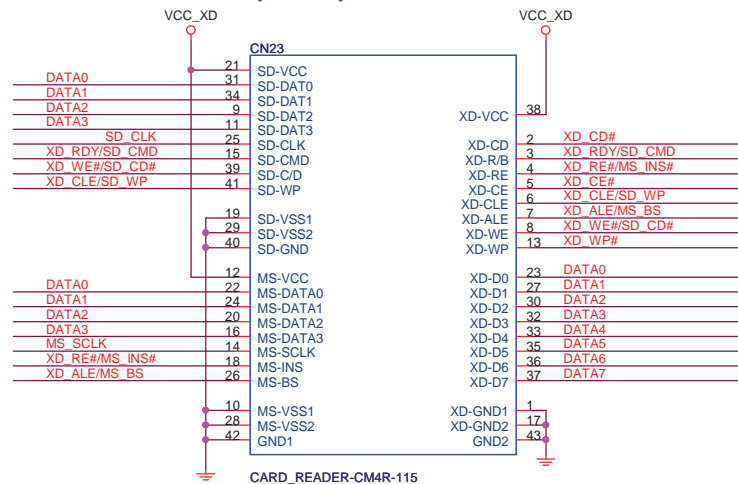
Sheet 24 of 47



## CARD READER Controller



## 4 IN 1 CARD READER (MMC)



Close to connector



4/20  
R589,R592 need to mount the bead SBY100505T121YN  
(CX05T121000 ) for EMI .

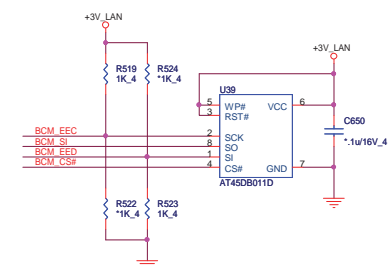
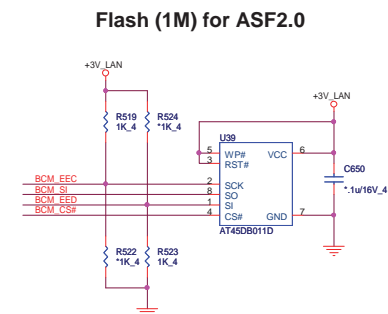
**Quanta Computer Inc.**

PROJECT : ZR9

## AU6437 CardReader

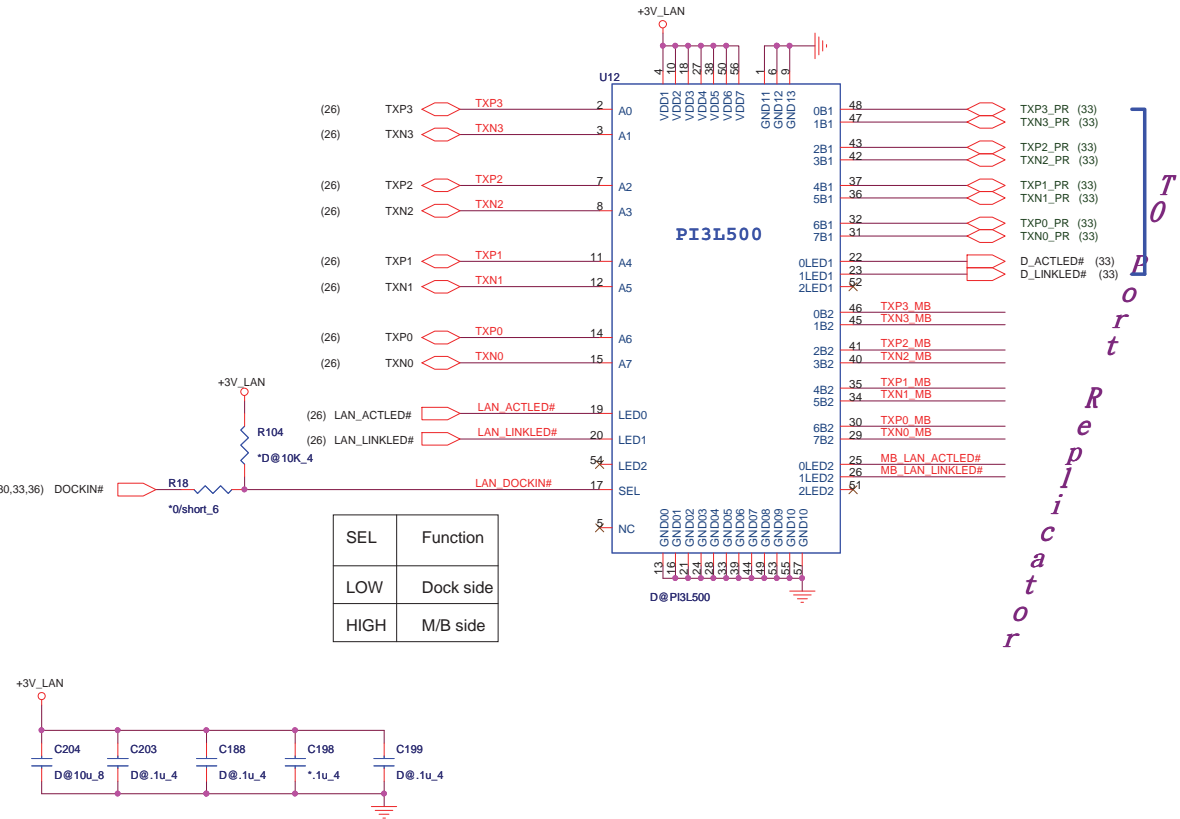


***WWW.AliSaler.Com***

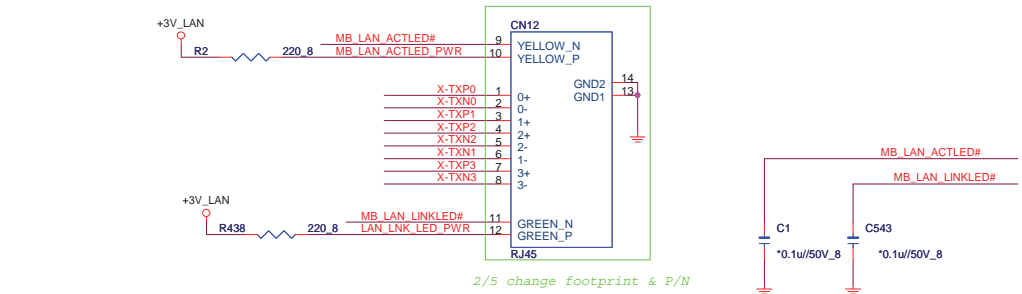




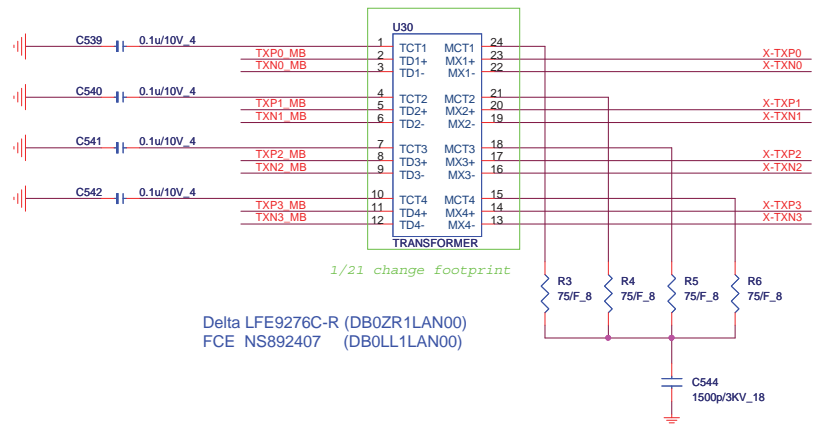
LAN SWITCH



RJ45(LAN)

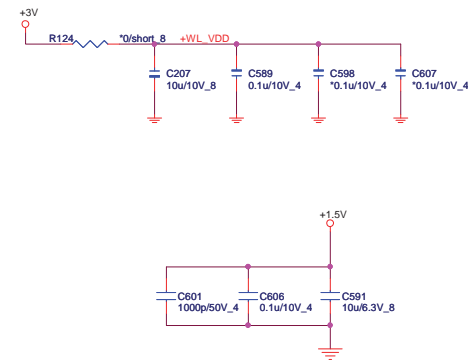
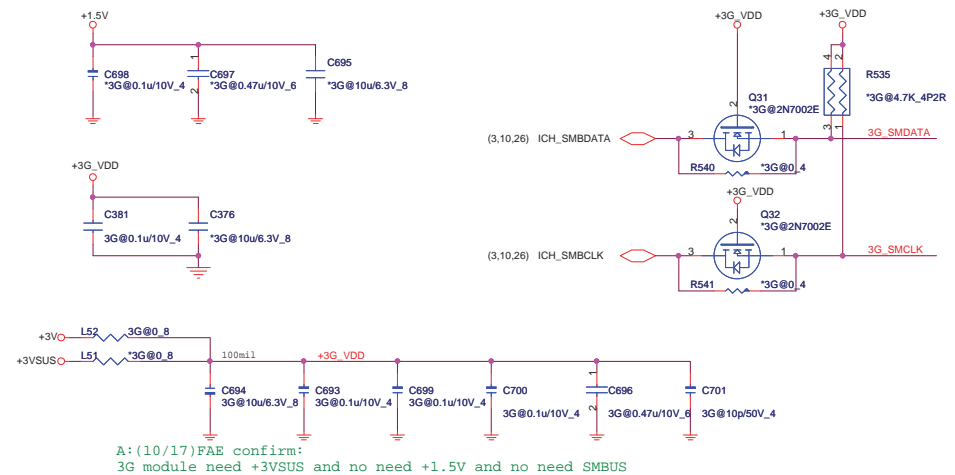
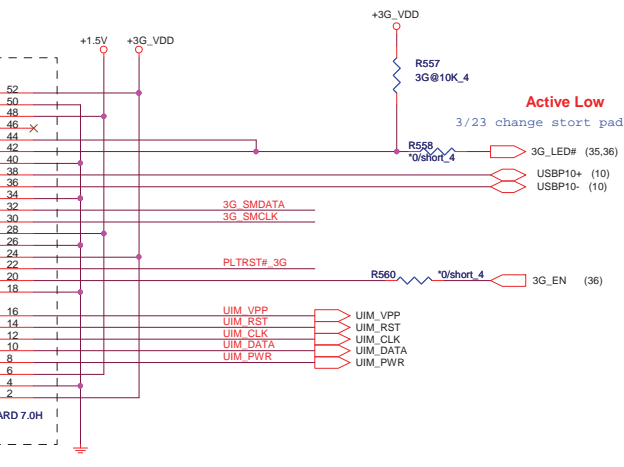
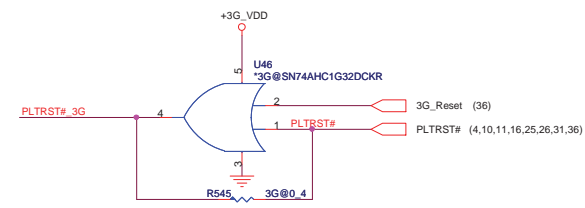
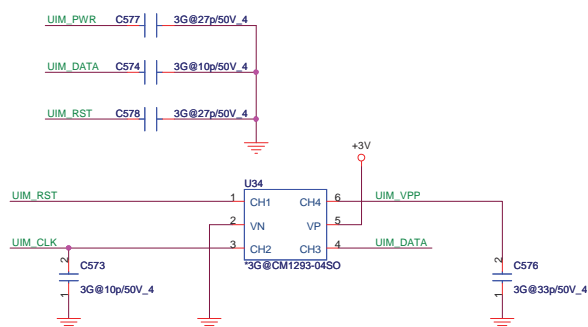


TRANSFORMER



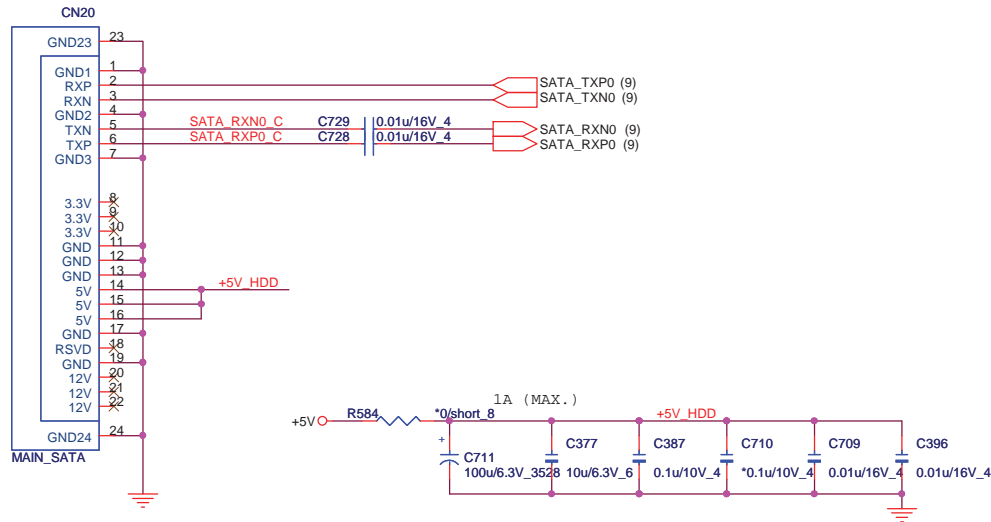


+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

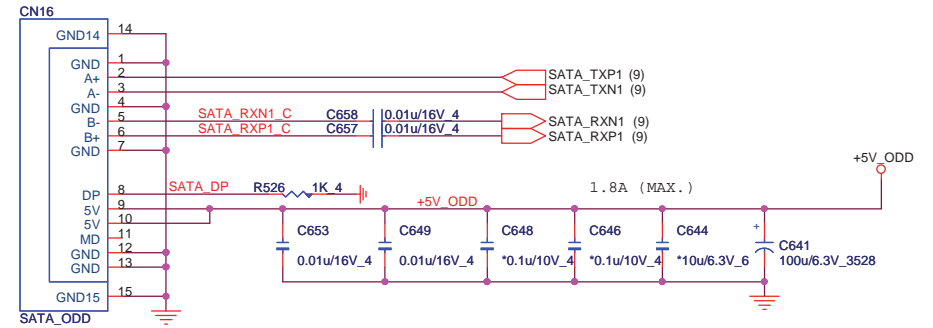
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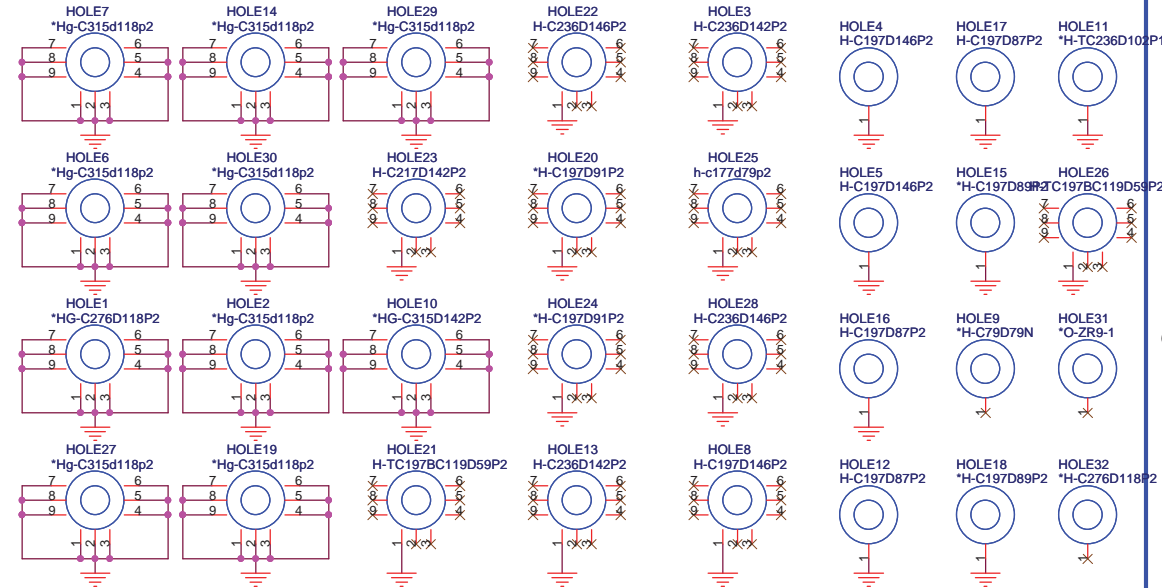
## SATA HDD(HDD)



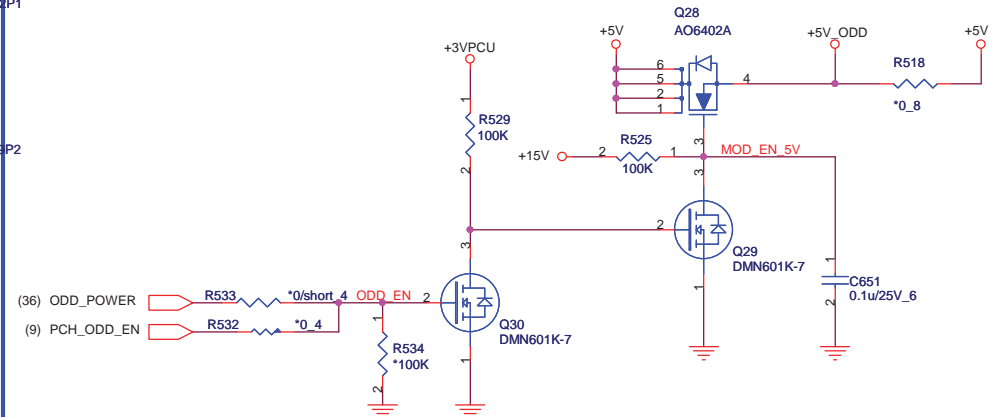
## SATA ODD (ODD)



## HOLE(OTH)

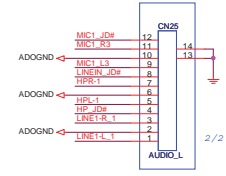
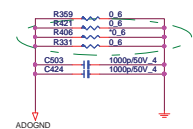
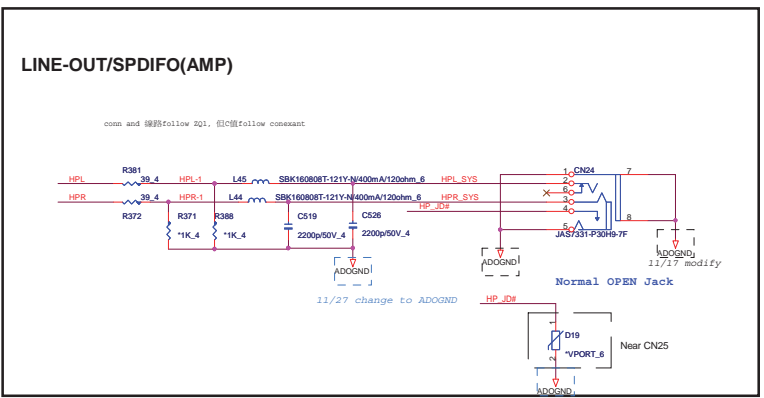
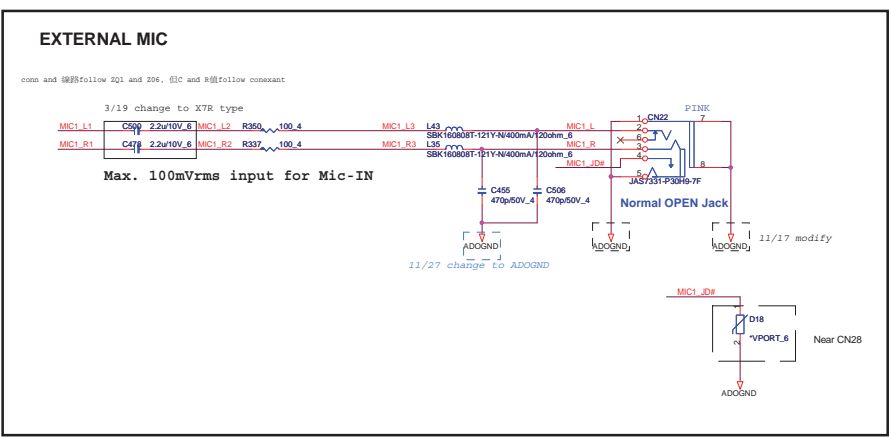
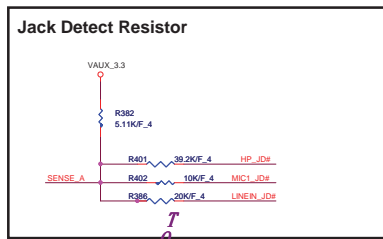
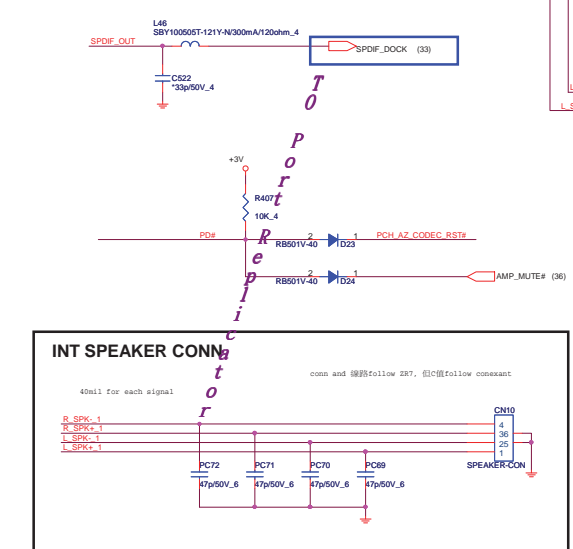
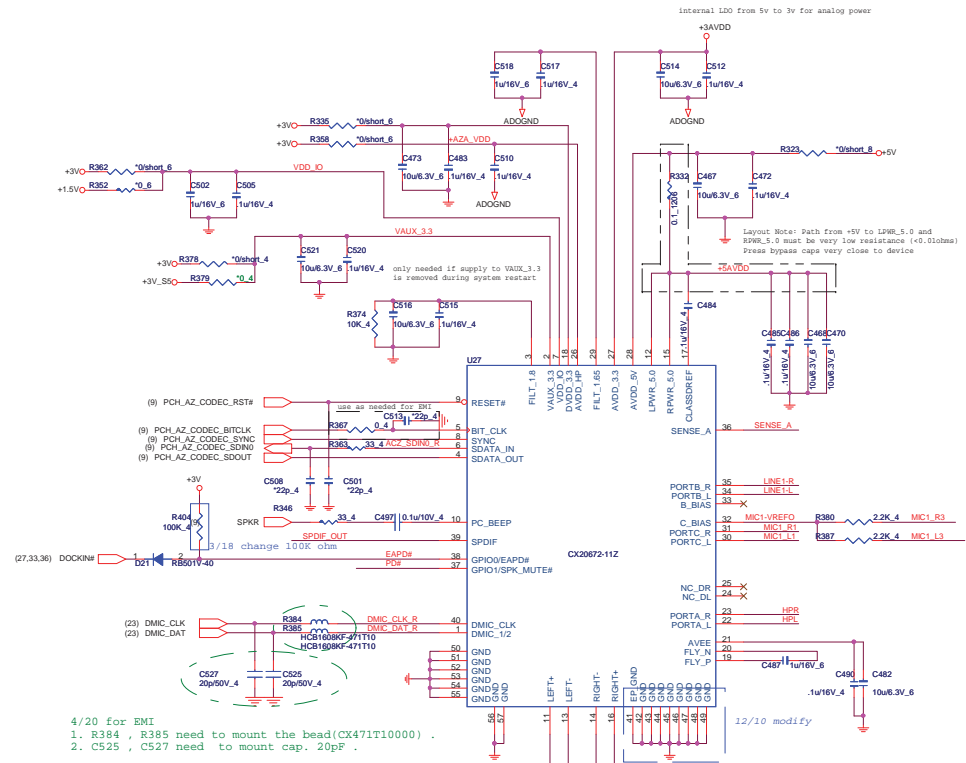


## ODD POWER(ODD)



Connect to PCH(GPIO21) pin Y9  
and EC pin28(GPIO53)

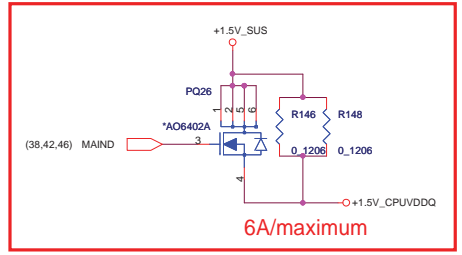
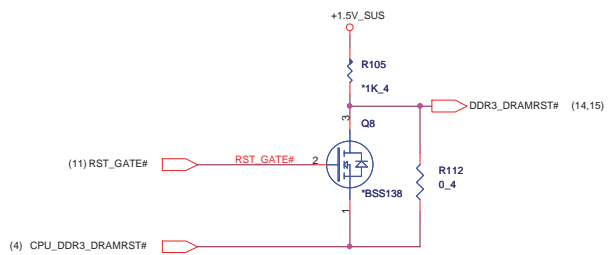
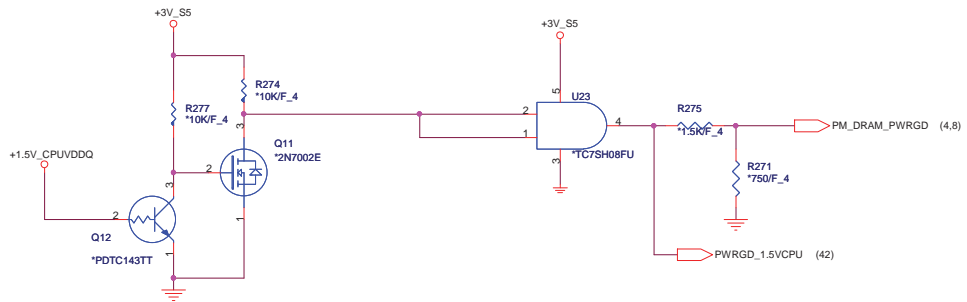
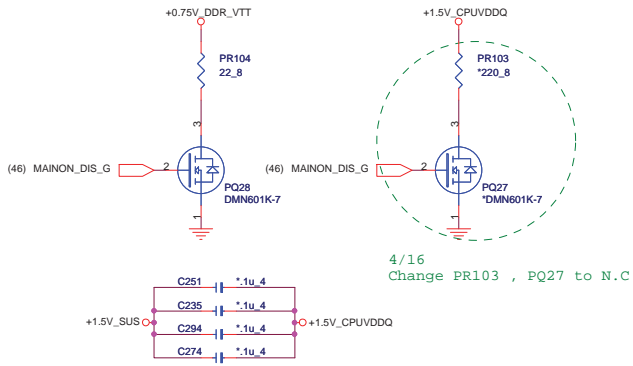
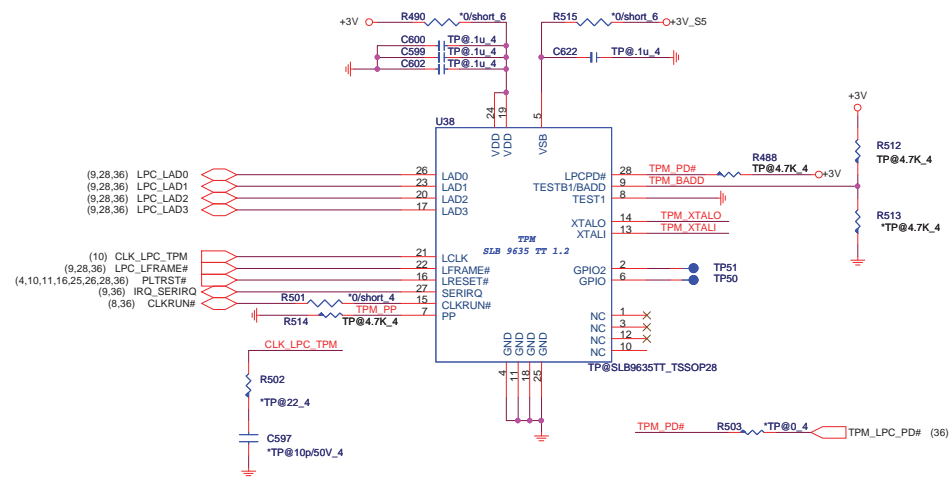






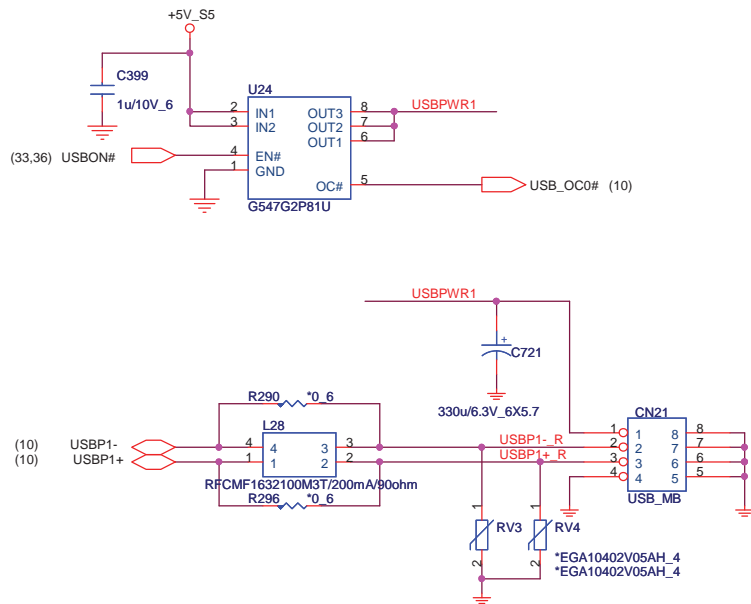
Trust Platform Module (Reserved)

	Resigser Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

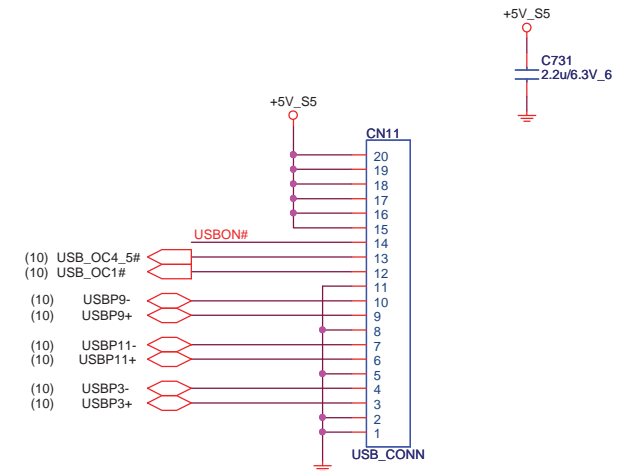




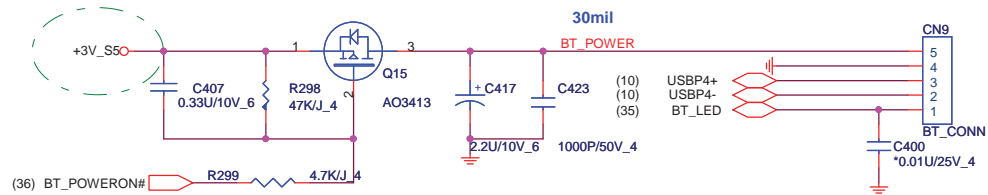
## USB PORT(USB)



### USB BOARD CONN(USB)



## BLUETOOTH CONNECTOR



4/16 modify power from +3V to +3V\_S5



**Quanta Computer Inc.**

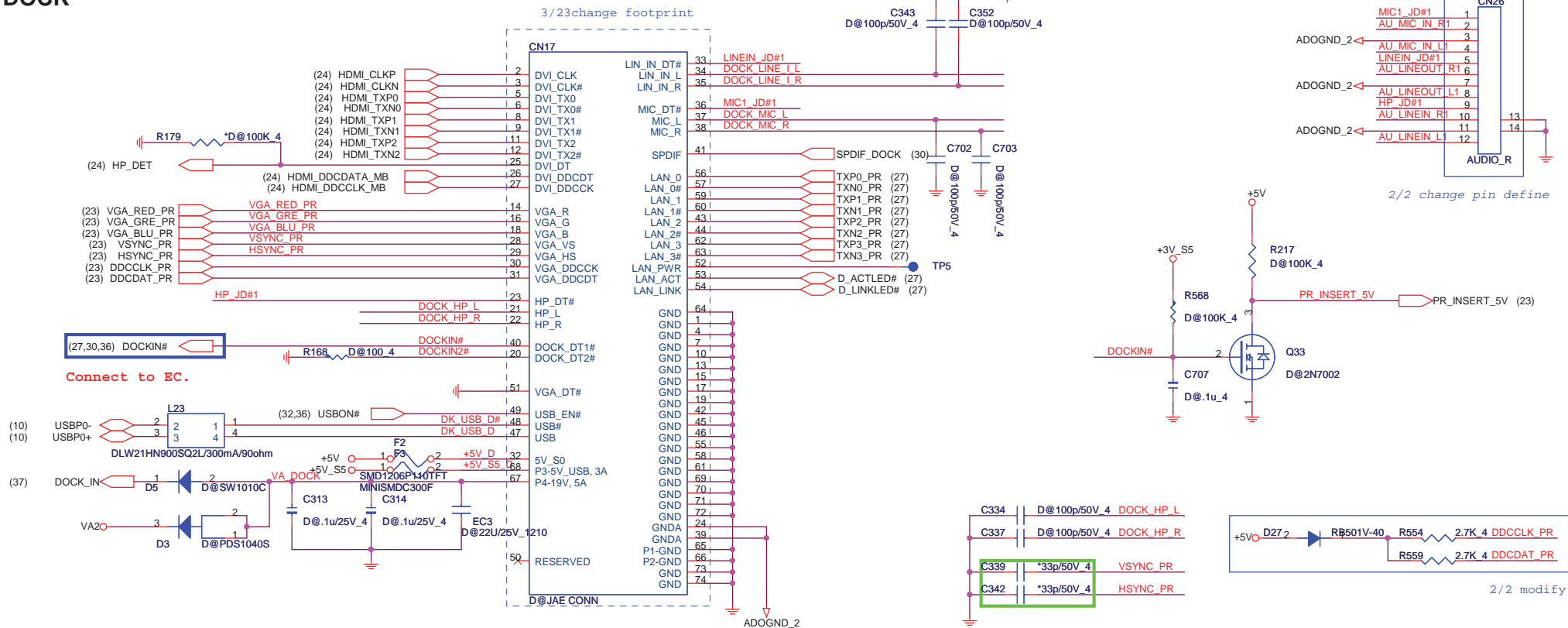
PROJECT : ZR9

BT/USB/USB DB

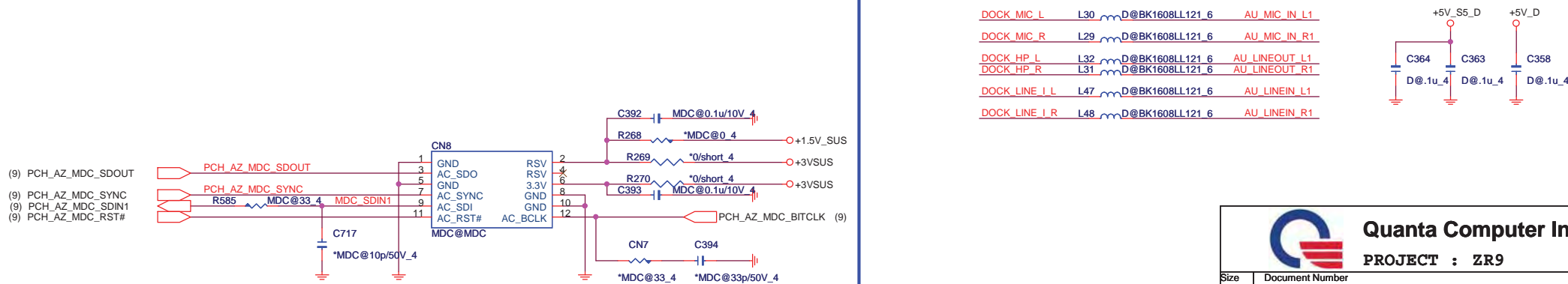
Size	Document Number	Rev
	<b>BT/USB/USB DB</b>	<b>1A</b>
Date:	Wednesday, May 05, 2010	Sheet 32 of 47



## CABLE DOCK

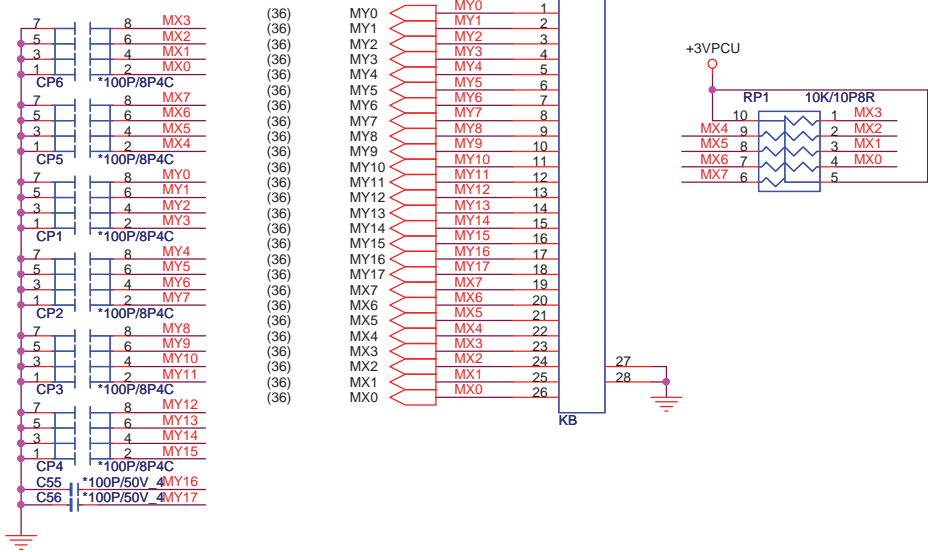


**MDC(MDM)**

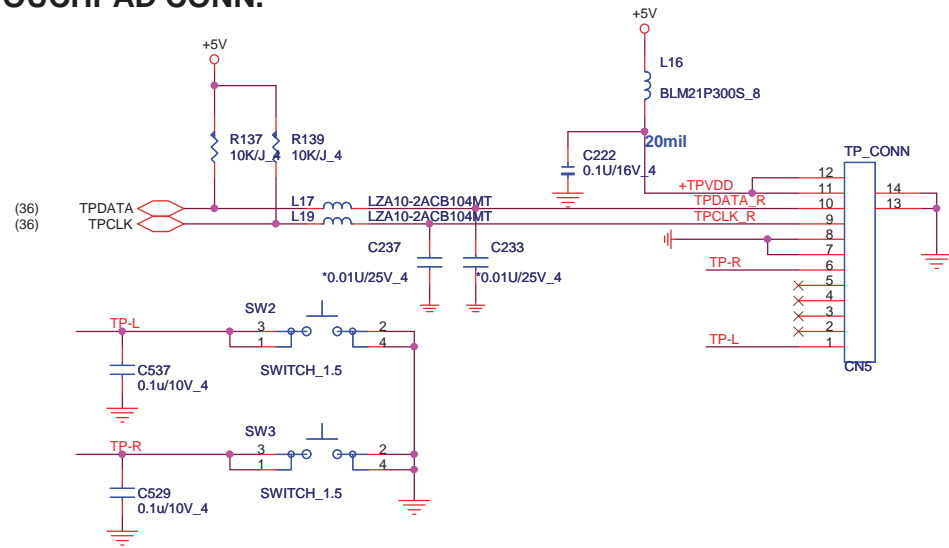




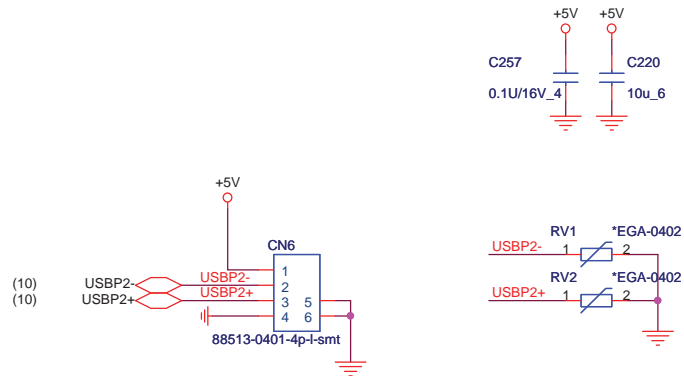
## INT K/B



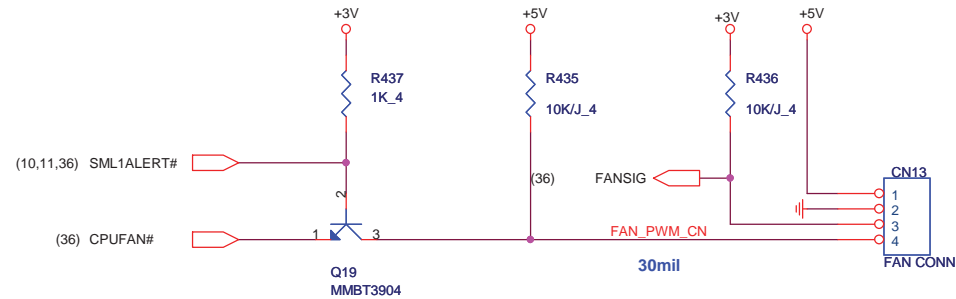
## TOUCHPAD CONN.



## Finger-Printer CONN.



## CPU FAN

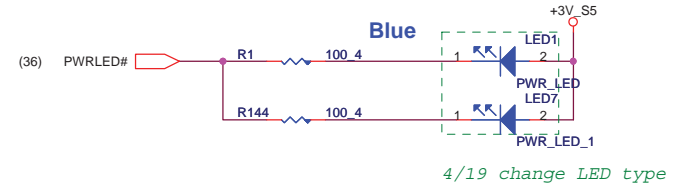
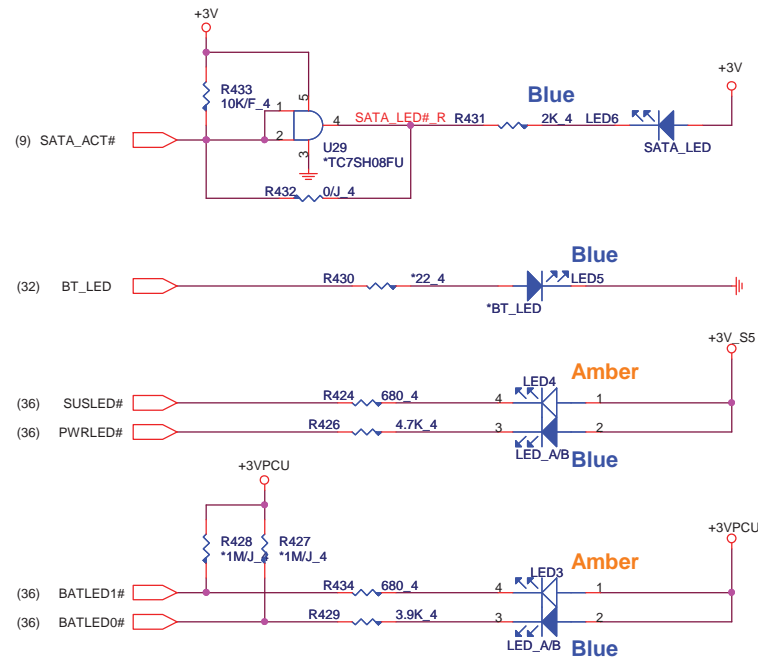


Quanta Computer Inc.  
PROJECT : ZR9

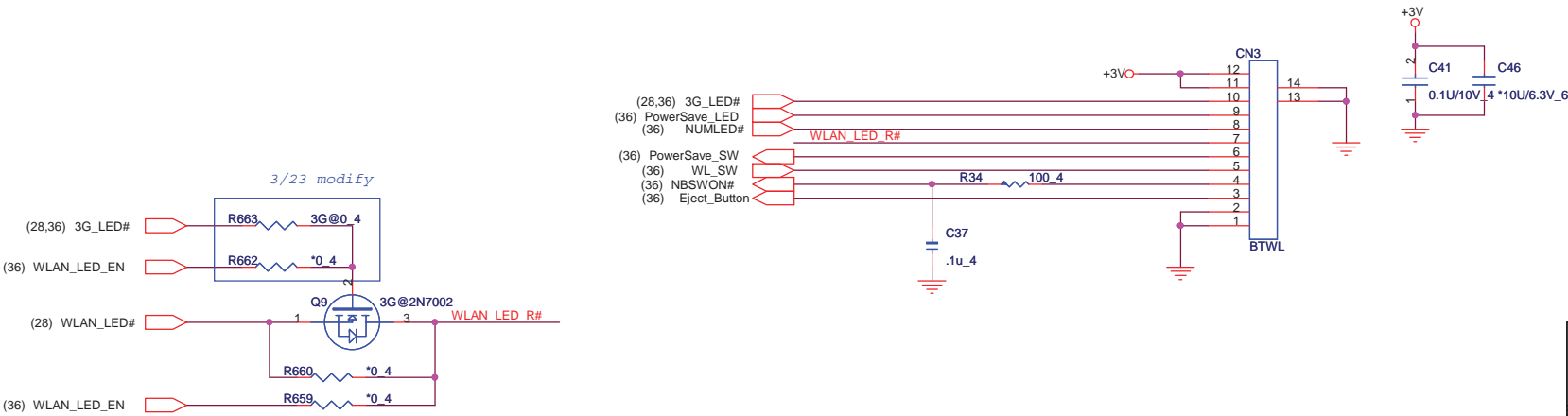
Size	Document Number	Rev
	KB/TP+FP/FAN	1A
Date:	Thursday, May 06, 2010	Sheet 34 of 47



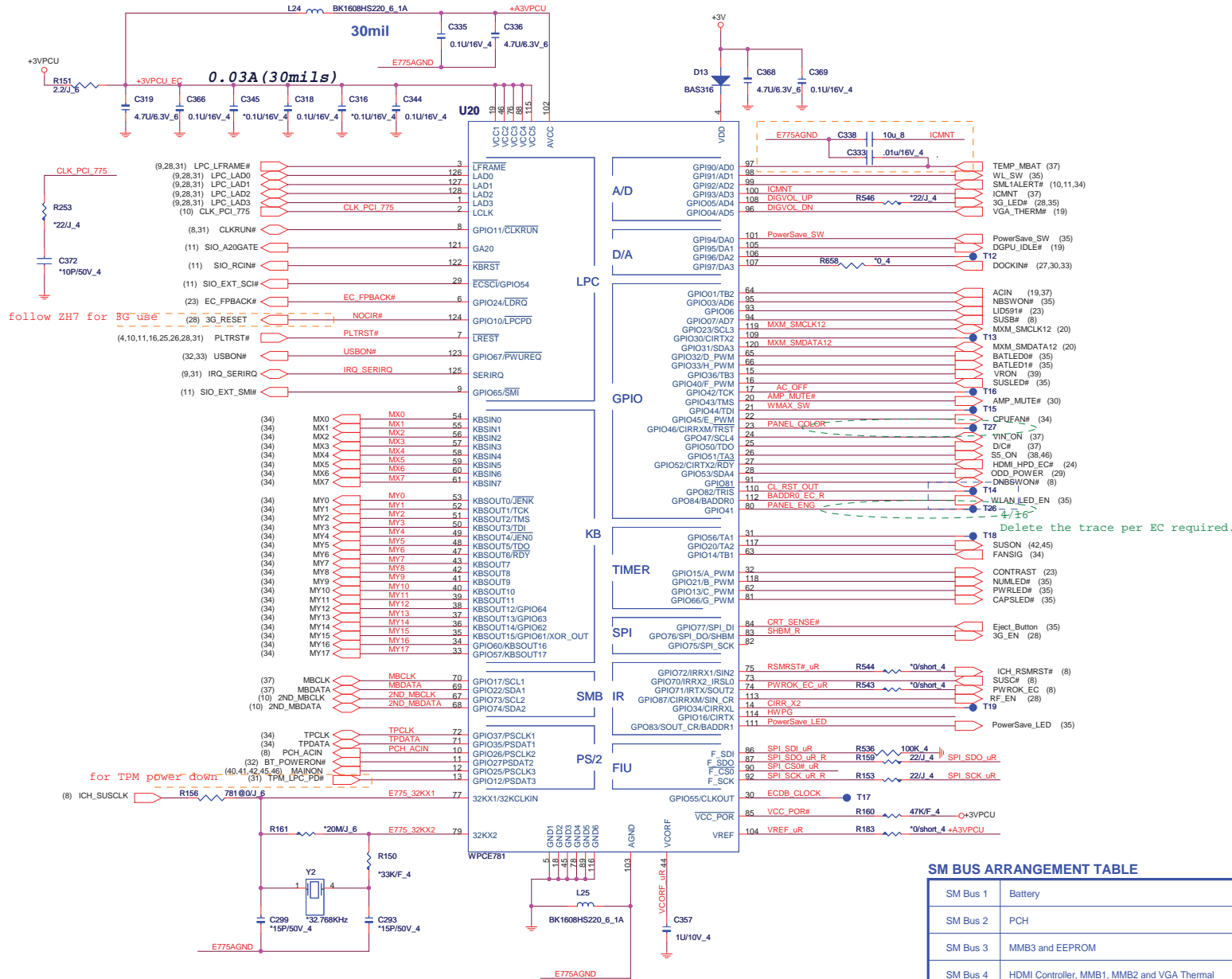
## M/B LED



## POWER D/B CONNECTOR







## SM BUS PU

## ACER ID

## SPI FLASH

1/13 Confirm by vendor mail :  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

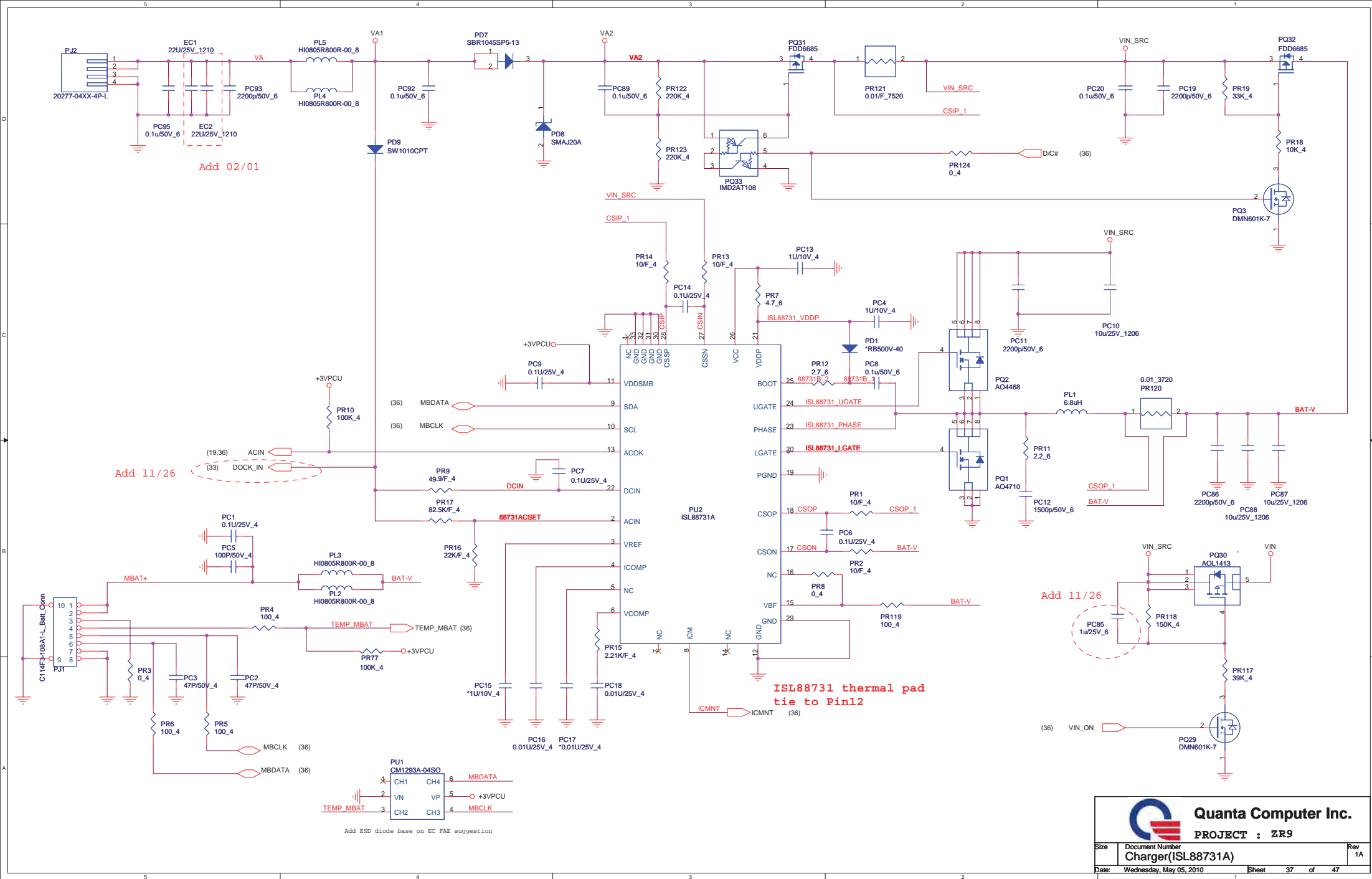
At 11/24 add  
Winbond W25Q16BVSSIG  
MXIC MX25L1606AM2C-15G  
EON EN25F16-100HIP  
AMIC A25L016

## HWPG

## INTERNAL KEYBOARD STRIP SET

## POWER-ON Switch





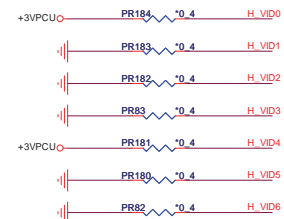




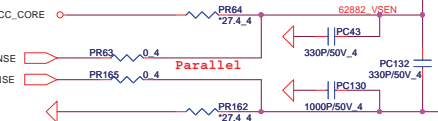
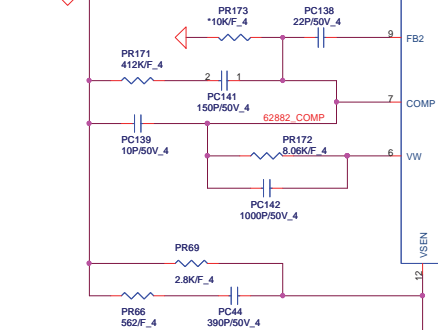
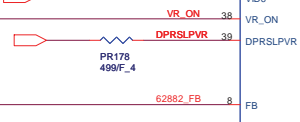
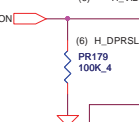
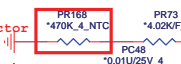


[PWM]

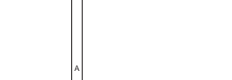
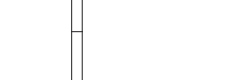
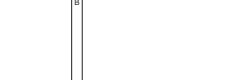
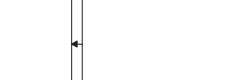
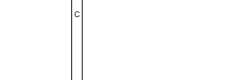
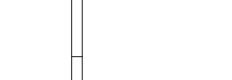
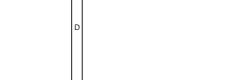
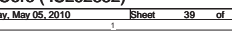
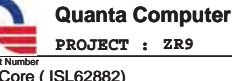
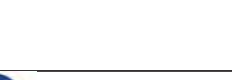
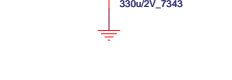
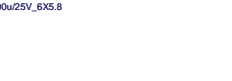
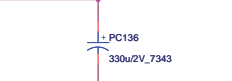
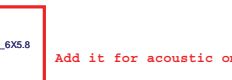
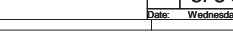
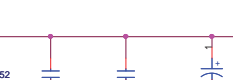
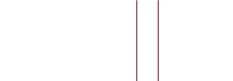
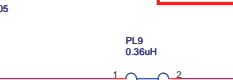
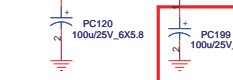
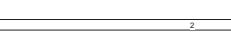
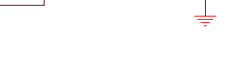
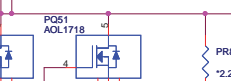
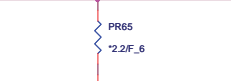
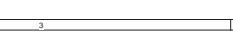
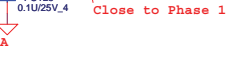
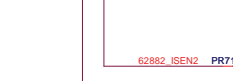
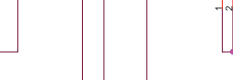
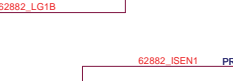
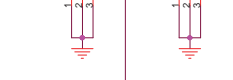
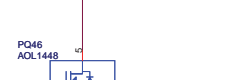
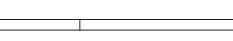
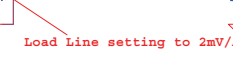
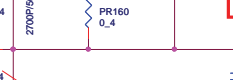
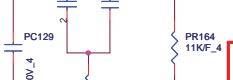
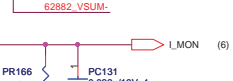
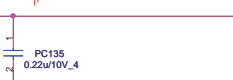
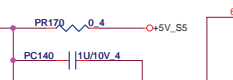
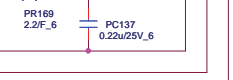
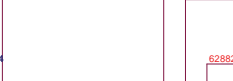
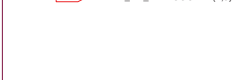
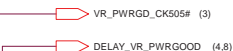
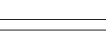
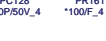
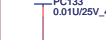
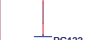
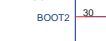
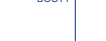
VID 1.2875V



Close to Phase 1 Inductor



change netname on 0419



Add it for acoustic on 4/19

20A

+VCC\_CORE

PC136

330u/2V\_7343

PC122

0.1u/50V\_6

PC124

4.7u/25V\_0805

PC123

4.7u/25V\_0805

PC120

100u/25V\_6X5.8

PC199

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

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PC120

100u/25V\_6X5.8

PC120

100u/25V\_6X5.8

PC120

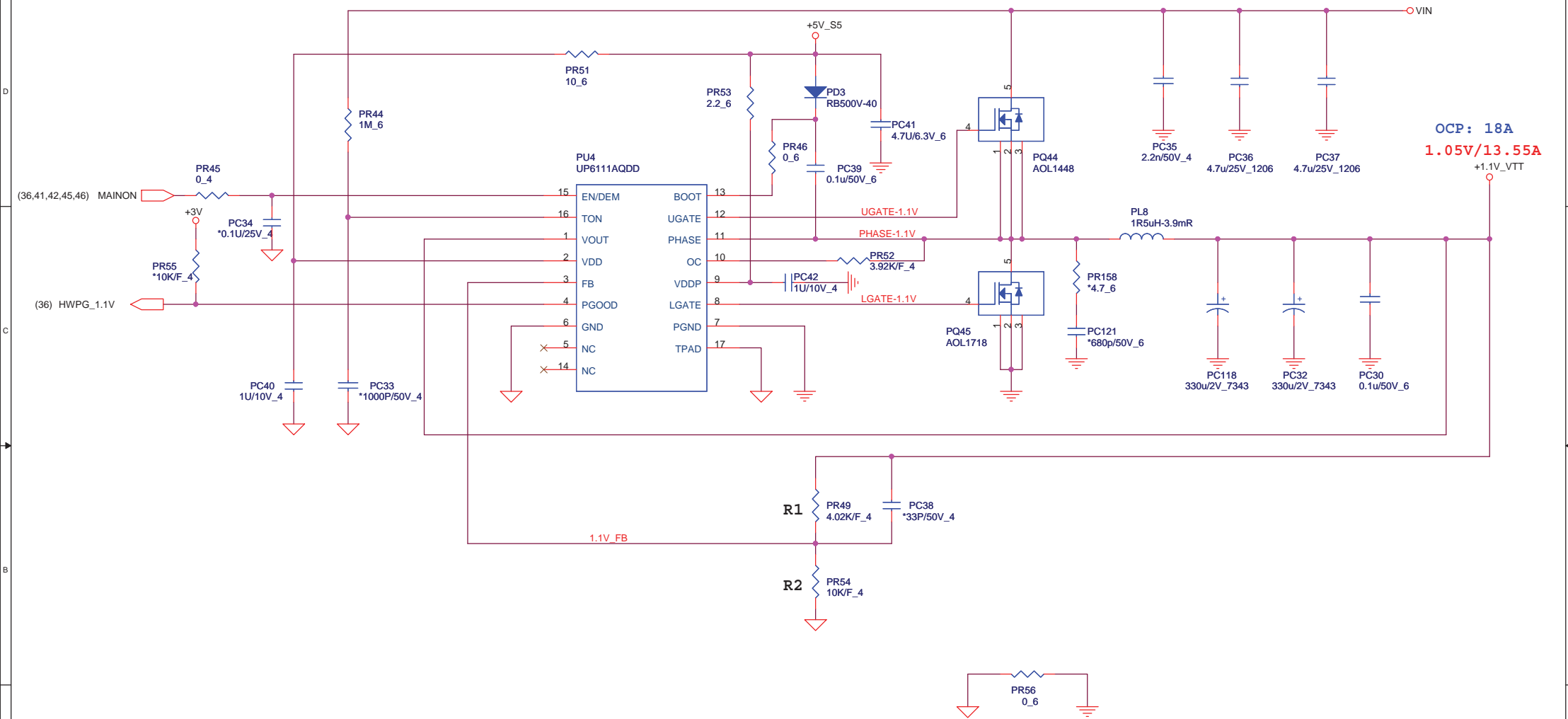
100u/25V\_6X5.8

PC120

100u/25V\_6X5.8



[PWM]



$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

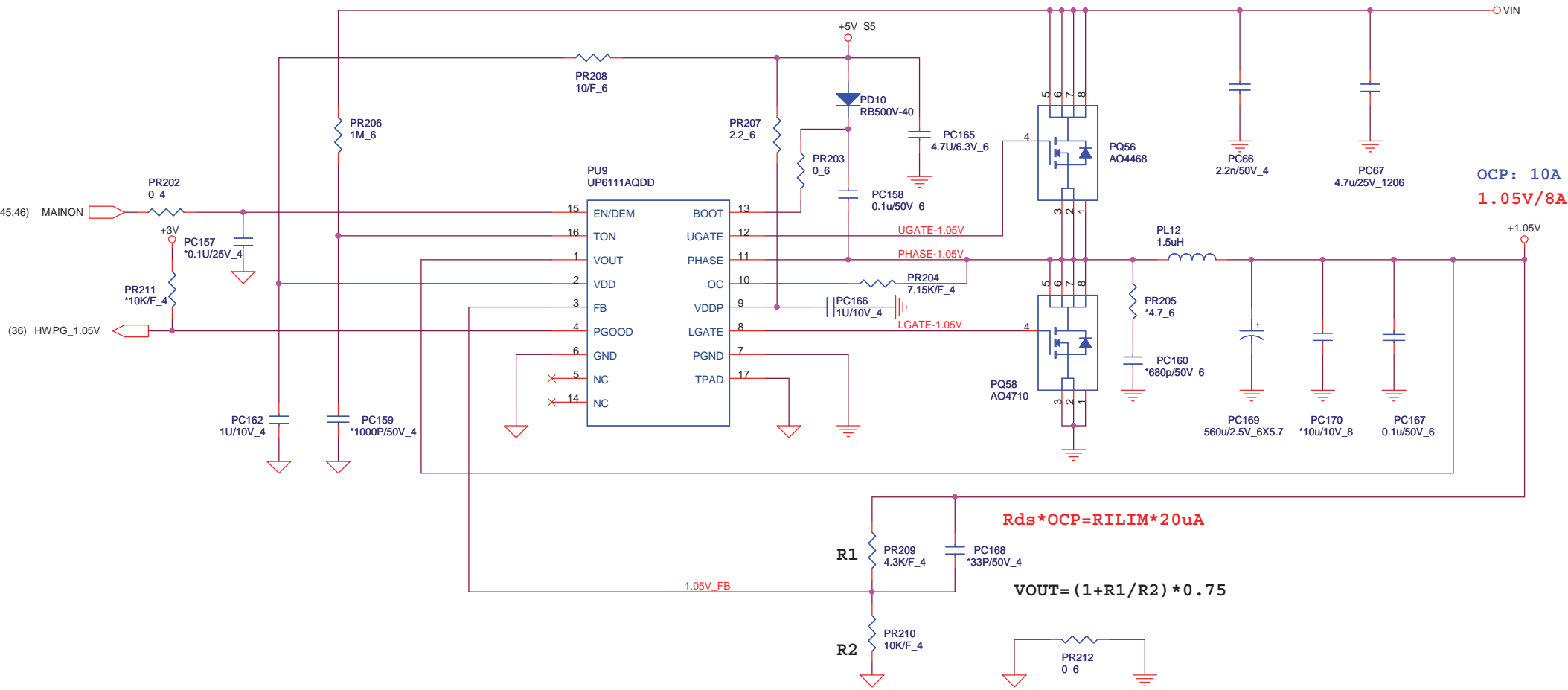
AOL1718  $R_{dson} = 3 \sim 4.3m\Omega$   
 $L(ripple\ current)$   
 $= (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19)$   
 $\sim 3.64A$   
 $4.3m \cdot 18 = RILIM \cdot 20uA$   
 $RILIM = 3.87K \quad \text{---} \quad 3.92K$



**Quanta Computer Inc.**  
**PROJECT : ZR9**


Size	Document Number	Rev
	<b>+VTT (UP6111A)</b>	1A
Date:	Wednesday, May 05, 2010	Sheet 40 of 47



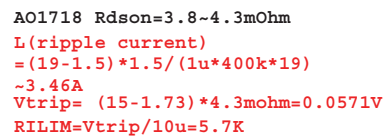


$TON = 3.85p * RTON * Vout / (Vin - 0.5)$   
 $Frequency = Vout / (Vin * TON)$   
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$   
 $Frequency = 1 / (0.0036767) = 272K$

AO4710 Rdson=11.7~14.2mOhm  
**L(ripple current)**  
 $= (19 - 1.05) * 1.05 / (1.5u * 272k * 19)$   
 $\sim 2.431A$   
 $14.2m * 10 = RILIM * 20uA$   
**RILIM = 7.1K --- 7.15K**

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR9</b>		Rev
		1A
Size	Document Number	
<b>VCCP 1.05V(UP6111A)</b>		
Date:	Wednesday, May 05, 2010	Sheet 41 of 47



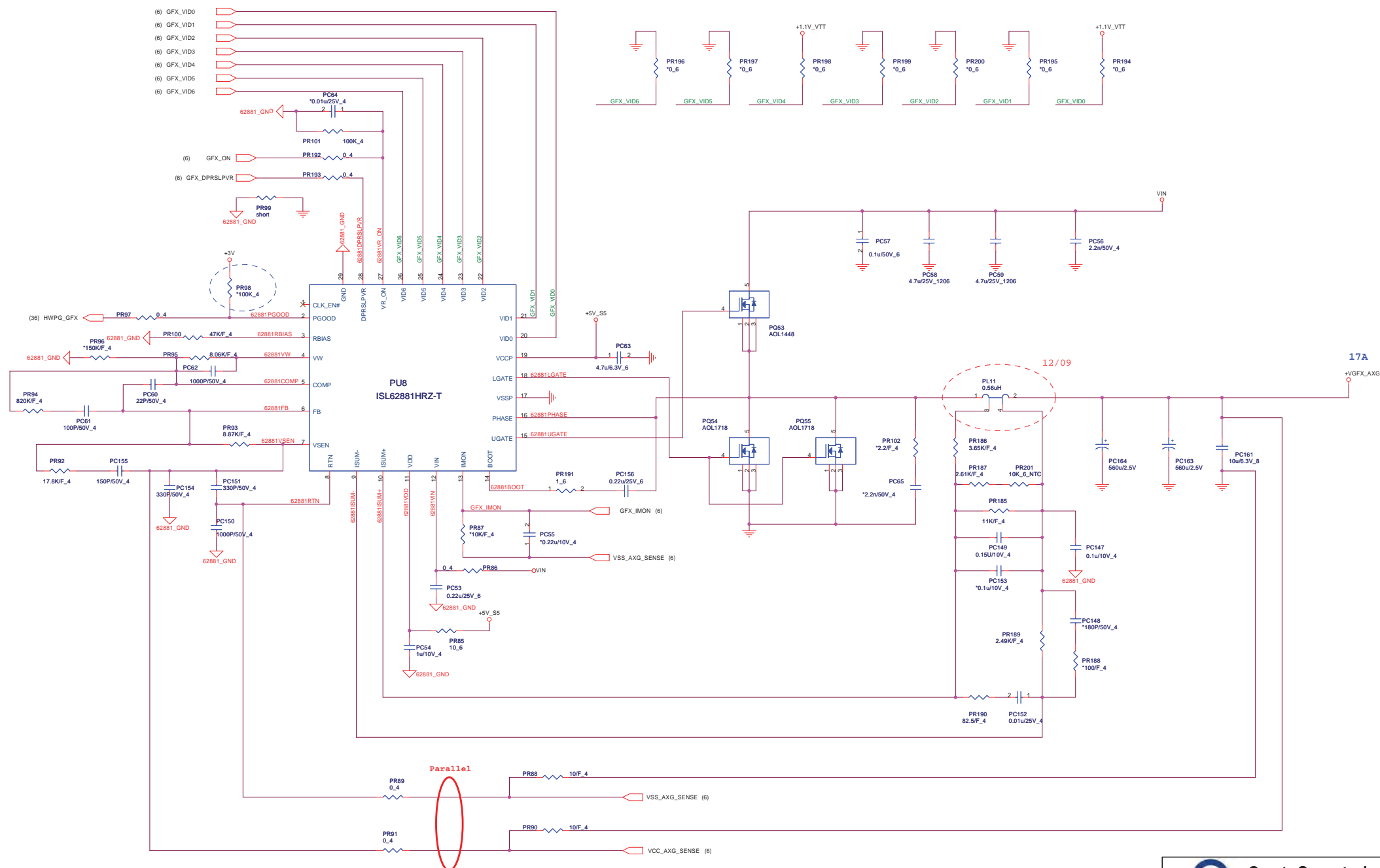


	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

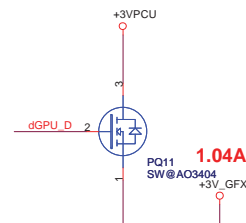
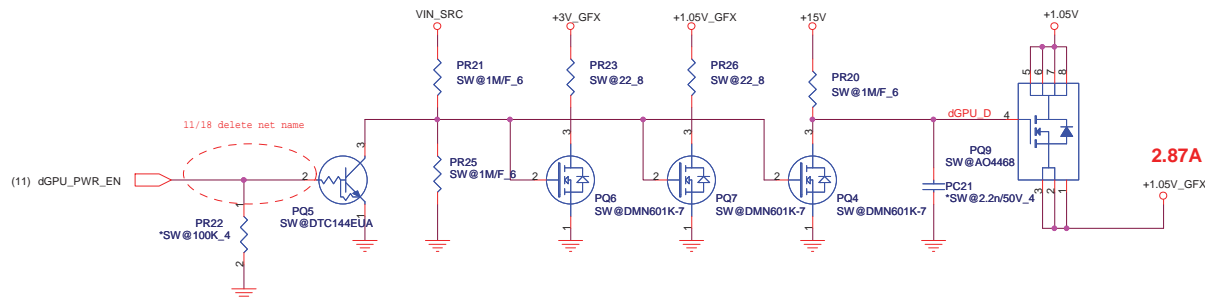
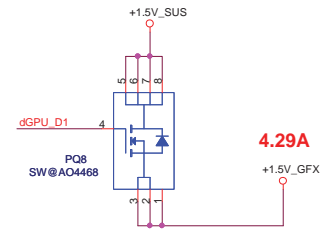
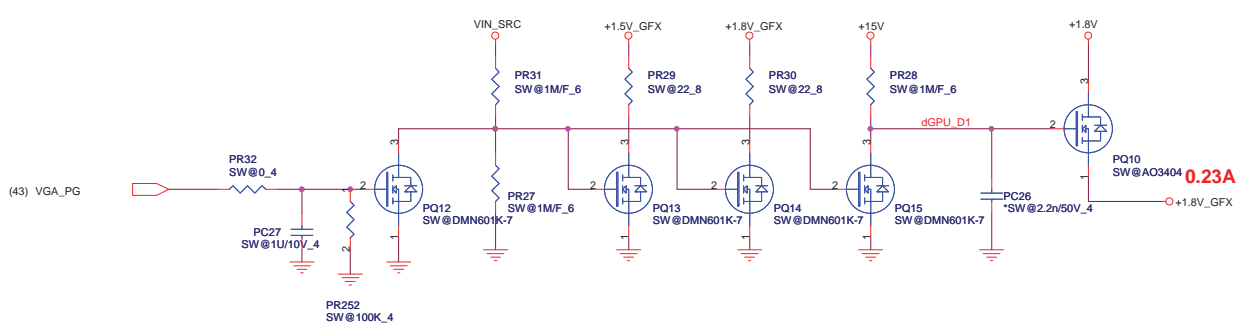
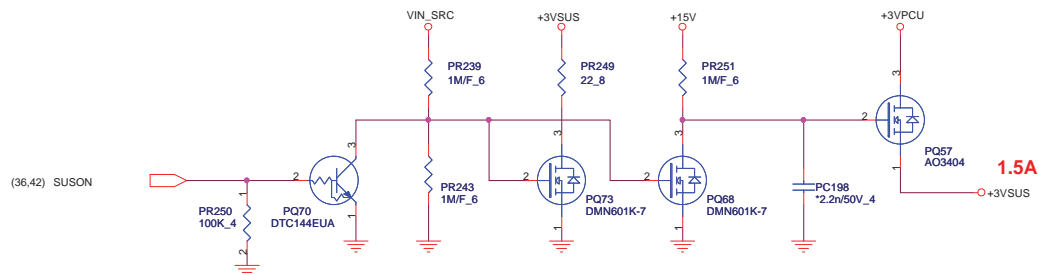
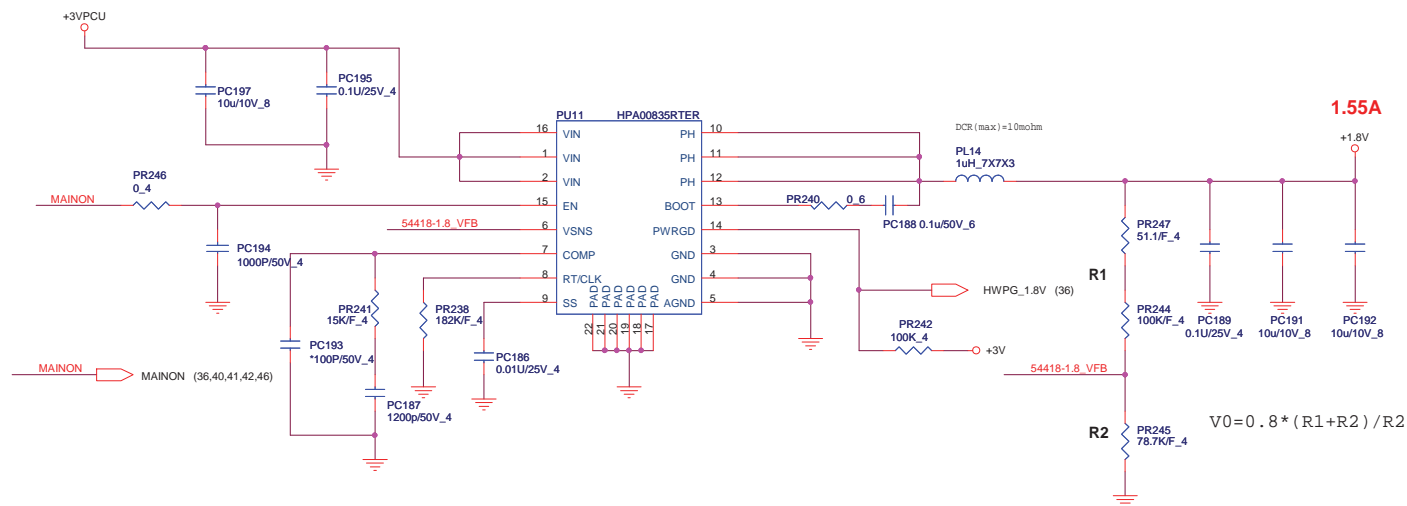


















Model	REV	DATE	CHANGE LIST
ZR9	A		
		20091117	page 10:delete R8145 & add C8407 & modify usb port define --> aim card to port 5 ,docking to port 0 page 34:modify CN7059 pin define page 30:modify speaker out circuit Evan Wang update Power circuit
		20091119	page 33 :cn9055 pin.67 change net name DCIN to Dock_IN page 18 Base on Design Guide , DVI should change to port E. Evan Wang update Power circuit
		20091124	page 4 :add R529,R232,R537,R527,R213,R524,R538,R536,R594,R528,R230 page 19 :delete R3515,R3514,Q3500,Q3501 page 24 :change net name MB_HDMI_DDCData ,Ma_HuMi_DocCLK to SDVo_CtrRL_Data ,DV0_CtrRL_Clk page 34 :delete R7451 & change R7442 to 1K , add C8031,C9053 page 30 :U9001 Pin.26 CT021change PD to AGND & add R13069,R228,R233 page 24 :delete R9798,R9810 page 35 :add LED7005,R7402,R7408 & modify CN7008 Pin define page 19 :add R3590 to PU +3V_GPX
		20091126	Evan Wang update Power circuit 1. Add PC9020(Iu/25V_6),2. PR9028 changes to 150K_4,3. PR9025 changes to 39K_4,4. Add P30308(SW6AOL1448),5.GPU_CORE solution change to MAX8722. page 35 :del LED7005,R7402,R7408 page 14 :J01M8000 SWAP PIN page 15 :J01M8999 SWAP PIN page 21 :U3502,U3509,U3503,U3508 SWAP PIN page 22 :U3504,U3500,U3501,U3507 SWAP PIN page 24 :U15 SWAP PIN page 27 :U45 SWAP PIN
		20091127	page 32 :Delete R395,R295,R297,R298,R363,R346,L28,L29,L32 page 16 :delete C3513,C3500,C3643,C3644,C3501 page 21 :delete C567,C569,C7,C560 page 22 :delete C565,C563,C20,C564 page 35 :add LED2,R7402 & modify CN7008 pin define page 23 :CN9049 modify pin define & change E pin page 32 :CN7008 modify pin define page 36 :U7020:L4 net name WLN_LED# change to U7020.L12 & add net name WLN_LED# on U7020.98 Evan Wang update Power circuit
		20091202	page 6 :del R8237 page 12:del R8268 & add R8432,R8433 page 30:del R228
		20091203	page 32:CN11 change pin define page 35:del D13,U7022 & add R13093,R12101 page 35:add R7406,LED7001 page 23:CN9049 change to 8 pin
		20091210	page 35:R7398,R7399,R7400R7402,R7403,R7404,R7405,R7406 chnage to 150 ohm page 35:add Q7027
		20091214	page 24:add R9802,R9795
		20100106	page 4: change R185 to NC page 8: change R395 to un-mount page 10: change C715,C714 to 33pf & add R508,R653,R654,R655,R656,R657 & for LAN SMBus Form SMB_CLK_M0,SMB_DATA_M0 to ICH_SMBCLK,ICH_SMBDATA & change high resistor 4.7k ohm R134,R135 close to chip side page 11: chnage dBPU_PWR_EN pin high resistor 10K un-mount page 18: change C595,C596 to 33pf page 23: V0A power add poly switch page 26: LAN SMBus change net name to ICH_SMBCLK,ICH_SMBData & C228,C229 to 33pf page 28: del net name RP_EN & R559 & R511 un-mount page 31: change R508 to NC page 33: Dock power add poly switch & R269,C392 un-mount page 35: change Q9 to N type & add R660,R659 page 36: add R658 Evan Wang update Power circuit
		20100125	page 30: add connector CN25 & change L29 , L30 , L31 , L32 , L47, L48 ,C531 , C530 to docking side page 33: add connector CN26 page 33: CN17 ADOGND change to ADOGND_2 Evan Wang update Power circuit
		20100201	page 23: add U91 page 33: CN26 ADOGND change to ADOGND_2 page 36: add R547 page 33: add R554,R559 & D27 page 33: Docking power add F2,F3 page 27: CN12 chnage footprint
		20100202	
		20100205	
		20100325	page 12: Add C530 to decrease CRT DAC ripple noise page 25: Change R589, R592 to lead for EMI require page 30: E478 , C590 change from 1uF to 2uF for WIC +H0+R quality page 30: R404 pull up to 100K for docking insert detect page 35: Change F0WLED5 power to +3V_Ss to prevent when AC go into power saving , power LED will turn on in Battery only. page 35: Modify SB/WiFi LED turn on behavior
		20100416	page 32 : Modify B/T power from +3V to +3V_Ss page 23 : 1. Change L1 to 0805 size 2. Change R12 , R13 from 0603 to 0402 page 31 : Change PR103 , PQ27 to W.C page 23 , 36 : Delete PANEL_COLOR and PANEL_ENG per EC requirement. page 41 : PR209 changes to 4.3K/F_4(CS24302PB07) page 37 : Mount PR11 and changes to 2.2_6(CS-2203F911) page 37 : Mount PC12 and changes to 1500p/50V_4(CH21506K915) page 43 : PR24 changes to 8Wx2_2_6(CS-2203F911) page 43 : PC24 changes to 8Wx1500p/50V_4(CH21506K814) page 35 : Change BXP power LED size from 0805 to 0603 and the quantity increase to two page 23 : Add Cap. C531 , C748-C752 for monitor test page 23 : Remove R12 , R13 and mount common mode choke L1 for EMI requirement page 25 : R589,R592 need to mount the bead s8V1005057121W(CX057121000 ) for EMI requirement page 30 : EMI suggested that R421 , R331 need to be mounted page 30 : R384 , R385 need to mount the bead(CX4711T1000) for EMI page 30 : C525 , C527 need to mount cap. 20pF for EMI
		20100420	